Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information

Program	M. Tech. All Branches
Class, Semester	First Year M. Tech., Semester I
Course Code	7IC501
Course Name	Research Methodology and IPR

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	---	30	20	50	100
		Credits: 3			

Course Objectives

1	To prepare students for undergoing research, identify and formulate the research problems, state the hypothesis, design a research layout, set a research process and methodology.
2	To enable student interpret the results, propose theories, suggest possible/alternative solutions, solve, and prove the solution adapted–logically and analytically, conclude the research findings.
3	To impart knowledge to analyze critically the literature and publish research in conferences, journals and to expose students to research ethics, IPR and Patents

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Demonstrate** a research solution in respective engineering domain using appropriate Engineering research process and research methodology.	Apply
CO2	**Device** feasible solution to a research problem in respective engineering domain based on economic, social and legal aspects using appropriate research procedures and practices.	Analyze
CO3	**Write** research publication, Dissertation, IPR and patent document.	Create

Module	**Module Contents**	**Hours**
I	**Engineering Research Process** Meaning of research problem, Sources of research problem, Criteria and Characteristics of a good research problem, Errors in selecting a research problem, Definition, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.	6
II	**Research Methodology** Problem statement formulation, resources identification for solution, Experimental and Analytical modelling, Simulations, Numerical and Statistical methods in engineering research. Hypothesis and its testing by different techniques: Z-test etc.,	6
III	**Research Methods** Uni and Multivariate Analysis: ANOVA, Design of Experiments/Taguchi Method, Regression Analysis. Software tools like spreadsheets. Processing and Analysis of Data: Processing Operations, Types of Analysis-Presentation and Interpretation of Data Editing, Classification and Tabulation-	7

Solapure 23-8-2023
Dr. S.S. Solapure

(SKD) 23/8/2023

23/8/23

Dr. R.S Desai 23/8/2023

	Interpretation. Analyse your results and draw conclusions.	
IV	**Research Practices** Effective literature studies approaches, critical analysis, Plagiarism, Research ethics, Mendeley - Reference Management Software. Research communication- Effective Technical Writing, Writing a research article for Journal/conference paper, Technical report, Dissertation/ Thesis report writing, Software used for report writing such as WORD, Latex etc. Presentation techniques for paper/report/seminar. Publishing article in Scopus/SCI/Web of science indexed journal or conference.	7
V	**Intellectual Property Rights (IPR)** Nature of Intellectual Property: Patents, Designs, Trade and Copyright, Ownership of copyright, Term of copyright, Technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. New developments in IPR, Traditional knowledge ,Various Case Studies.	7
VI	**Patents** Patent Rights: Scope of Patent Rights. Various Patent databases. Geographical Indications. Procedure for grants of patents, Patenting under PCT. Licensing and transfer of technology. Administration of Patent System. Introduction to International Scenario: WIPO, TRIPs, Patenting under PCT	6

	Textbooks
1	Kothari C. R, "Research Methodology", 2nd Edition, New Age International, 2004
2	Melville Stuart and Goddard Wayne, "Research Methodology: An Introduction for Science & Engineering Students" Juta and Company Ltd, 2000.
3	Kumar Ranjit, "Research Methodology: A Step-by-Step Guide for beginners", SAGE Publications, 4th Ed.-2014.
	References
1	Merges Robert, Menell Peter, Lemley Mark, "Intellectual Property in New Technological Age", ASPEN Publishers, 2016.
2	Ramappa T., "Intellectual Property Rights Under WTO", S. Chand, 2008
3	Mayall, "Industrial Design", McGraw Hill, 1992.
4	Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007
5	Deepak Chopra and Neena Sondhi, Research Methodology : Concepts and cases, Vikas Publishing House, New Delhi
	Useful Links
1	NPTEL :: General - NOC:Introduction to Research
2	Introduction to Research - Course (nptel.ac.in)
3	Qualitative Research Methods And Research Writing - Course (nptel.ac.in)
4	https://onlinecourses.swayam2.ac.in/ntr21_ed23/preview - Academic Research & Report Writing
5	https://www.scopus.com/search/form.uri?display=basic#basic
6	https://onlinecourses.nptel.ac.in/noc21_ge12/preview - Qualitative Research Methods And Research Writing
7	https://onlinecourses.nptel.ac.in/noc21_hs44/preview - Effective Writing
8	https://webofscienceacademy.clarivate.com/learn

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9	https://onlinecourses.swayam2.ac.in/ntr21_ed23/preview - Academic Research & Report Writing
10	https://nptel.ac.in/courses/121/106/121106007/
11	https://www.wipo.int/about-wipo/en/

CO-PO Mapping						
	Programme Outcomes (PO)					
	1	**2**	3	4	5	6
CO1	3		1			
CO2			2	3	2	
CO3		3		2		2

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Solapur
28-8-2023
DE.S.S.Solapure
Associate Professor (IT)
Dept.

Walchand College of Engineering, Sangli *(Government Aided Autonomous Institute)*					
AY 2023-24					
Course Information					
Programme	M.Tech. Electronics Engineeing				
Class, Semester	First Year M.Tech., Sem I				
Course Code	7EN501				
Course Name	Advanced Digital Signal Processing				
Desired Requisites:	Signals and Systems, Digital Signal Processing				
Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives	
1	To illustrate the concepts of Advanced Signal Processing
2	To explain the different techniques for design of filters and multirate systems
3	To enable the students for the design and development of Adaptive DSP systems

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Explain the basic and advanced signal processing concepts	Discuss
CO2	Design FIR and IIR filters with given specifications	Design, Solve
CO3	Analyse the various algorithms related with multirate DSP	Analyze
CO4	Illustrate adaptive signal processing algorithms	Demonstrate

Module	Module Contents	Hours
I	**Review of Digital Signal Processing** Discrete Time Signals and systems, LTI Systems, Basic Signal Processing Operations, Discrete Time Systems-Classification, impulse and step responses, phase and group delays. Time domain and frequency domain characterization of LTI discrete time systems, Z Transform, Transfer function	8
II	**DSP Structures** Block Diagram Representation, Equivalent Structures, Basic FIR Digital Filter Structures, Basic IIR Digital Filter Structures, All pass Filters, Tuneable IIR Digital Filters, IIR Tapped Cascaded Lattice Structures, FIR Cascaded Lattice Structures, Parallel All pass Realization of IIR Transfer Functions	6
III	**DFT Computation Techniques** DFT-Definition and properties, symmetry properties, Circular convolution, Computation of DFT, Decimation in time (DIT) and Decimation in Frequency (DIF) Fast Fourier transform (FFT) algorithms , Linear filtering using FFT- overlap add, overlap save methods, Goertzel Algorithm	6

IV	**Filter Design Technique** Bilinear Transformation Method of IIR Filter Design, Design of Low pass IIR Digital Filters, Design of High pass, Band pass and Band stop IIR Digital Filters, Spectral Transformations of IIR Filters, FIR Filter Design Based on Windowed series, Design of Digital Filters with Least-Mean-Square Error, Constrained Least-Square Design of FIR Digital Filters	8
V	**Multi-rate Signal Processing** The Basic Sample Rate Alteration Devices, Filters in Sampling Rate Alteration Systems, Multistage Design of Decimator and Interpolator, The Poly phase Decomposition, Arbitrary-Rate Sampling Rate Converter, Digital Filters Banks, Two-Channel Quadrature-Mirror Filter bank	6
VI	**Introduction to adaptive signal processing** Introduction to Adaptive Filters, Steepest descent technique, LMS algorithm-Convergence analysis, Learning curve, SVD	6

Text Books	
1	Sanjit K. Mitra, "Digital Signal Processing – A Computer based approach", Tata McGraw-Hill, 4th Edition , 2013
2	Bernard Widrow, Samuel D. Stearns "Adaptive Signal Processing,", Prentice-Hall, Englewood Cli, NJ, 1985
References	
1	J. G. Proakis, Dimitris K Manolakis, "Advanced Digital Signal Processing Principals, Algorithms and Applications,", Pearson,2007
Useful Links	
1	NPTEL Lectures

CO-PO Mapping

	Programme Outcomes (PO)														
	1	2	3	4	5	6									
CO1			2												
CO2						1									
CO3				2											
CO4															

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. I
Course Code	7EN502
Course Name	Embedded System Design
Desired Requisites:	Microprocessors / Microcontrollers, Computer Programming

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives

1	Understand ARM processor core architecture with several features of peripherals available on various embedded Cortex- M processors
2	Understand interrupts and its programming with peripherals
3	Develop small embedded system by using the ARM processor core based systems and application software for it.
4	Use EDA tools to design embedded system.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**illustrate** Cortex M3 / M4 processor architecture and its features	Understand
CO2	**apply** programming skills to develop algorithm for peripherals and interrupts	Apply
CO3	**develop** embedded system software.	Create
CO4	**design** and develop embedded systems based applications	Create

Module	**Module Contents**	**Hours**
I	**ARM Cortex –M Architecture and Programming** ARM Cortex M3 / M4 Architecture, Registers, CPU status, Clock generation, Memory organization, Instruction Set, Programming model – Registers, Operation Modes, Embedded C Programming	6
II	**Cortex M CPU Interrupts** Nested Vectored Interrupt Controller (NVIC), Vector table, Interrupt priorities, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency, Start-up files, initialization of peripherals interrupts, Interrupt routines programming	8
III	**ARM Peripherals and Programming** On chip peripherals, GPIO, RTC, Watchdog, ADC, DAC, Timer, PWM, Memory, DMA programming, External Peripheral Interfacings and their programming.	8
IV	**Communication and Programming** Communication Peripherals: UART, I2C, I2S, and SPI , CAN BUS programming, LIN bus programming, Drivers for serial port communication	8
V	**Algorithm Designing and Debugging** State Machine based Embedded Programming, Writing initialisation programs, Debugging techniques, Debugging with JTAG, Debugging with UART port, open source tools for software development	6
VI	**Embedded System Implementation** Development Environment, Debugging Techniques, Designing, Manufacturing and Testing steps and issues.	4

Textbooks	
1	Joseph Yiu, “The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors”, Newnes; 3rd edition
2	Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
3	Yifeng Zhu, “Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C”, E-Man Press LLC
4	"Introduction to Microprocessor Based Systems Using the ARM Processor" by Kris Schindler
References	
1	Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2	Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3	Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
4	Technical references and user manuals of respective controller
Useful Links	
1	https://nptel.ac.in/
2	https://in.coursera.org/
3	https://www.nxp.com/
4	https://www.arm.com/

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2	3													
CO3		3			3									
CO4			3											3
1: Low, 2: Medium, 3: High														

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher’s assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information

Programme	MTech. Electronics
Class, Semester	First Year MTech., Sem I
Course Code	7EN503
Course Name	Digital VLSI Design
Desired Requisites:	Digital Techniques

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives

1	To explain the relevance of CMOS technology in implementing digital circuits
2	To discuss in details various logic styles (static, dynamic) in implementing CMOS circuits and the effect of choosing a particular style on device performance from delay, power and area point of view.
3	To develop the architectures of few data-path designs (system building blocks) and an insight into extracting the functionality of displayed CMOS circuit
4	To motivate the students to develop lifelong/self-learning attitude

Course Outcomes (CO) with Bloom's Taxonomy Level

After the completion of the course the student should be able to

CO1	**Apply** the analytical expressions involving physical parameters, process parameters and electrical parameters to characterize the MOS transistors **by taking into account** the fundamental principles involved with MOS devices	Illustrate
CO2	**Analyze** static and dynamic CMOS circuits numerically to compute the various device parameters and circuit performance parameters computational skills.	Develop
CO3	**Analyze** static and dynamic CMOS circuits numerically to compute the various device parameters and circuit performance parameters	Analyze
CO4	**Select** an appropriate logic style to design submicron MOS transistor based circuits using logical, analytical and computational skills.	Design
CO5	**Design** the self timed CMOS circuits, and synchronous circuits with built-in arbiters, synchronizers	Develop

Module	**Module Contents**	**Hours**
I	**MOS Transistor** MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling	4

II	**CMOS Inverter** CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter	6
III	**Combinational Static Logic Design** Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance	8
IV	**Combinational Dynamic Logic Design** Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs	6
V	**Sequential Logic Design** Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers	8
VI	**Timing Issues in Digital Circuits** Timing Classification, Synchronous Design (Clock skew, Jitter, Clock Distribution), Self-Timed Circuits Design, Synchronizers and arbiters, Using PLL for clock synchronization	7

Text Books	
1	1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits, A System Perspective*", Pearson Education, Second Edition, First Indian Reprint, 2003.
2	Neil Weste, Kamran Eshraghian "*Principles of CMOS VLSI Design*", Addison Wesley/Pearson Education, 2010
References	
1	Kamran Eshraghian, Pucknell and Eshraghian "*Essentials of VLSI Circuits and Systems*", , Prentice-Hall (India), 2008
2	Sung-Mo Kang, Yusuf Leblebici "*CMOS Digital Integrated Circuits: Analysis and Design*", McGraw Hill Education (India), Third Edition, 2003
3	Neil Weste, David Harris, Ayan Banerjee "*CMOS VLSI Design*", Pearson Education, 2008
Useful Links	
1	NPTEL Lectures

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1				2											
CO2						1									
CO3						1									
CO4			2												
CO5			1												
CO6						2									

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem I
Course Code	7EN551
Course Name	Advanced Digital Signal Processing Lab
Desired Requisites:	Digital Signal Processing

Teaching Scheme (Hrs)		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2Hrs/week				
Interaction	-	**Credits: 1**			

Course Objectives

1	To make students familiar with the most important methods in DSP, including digital filter design, transform-domain processing and importance of Signal Processors.
2	
3	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Apply signal processing to various areas such as speech and	Apply
CO2	audio processing, image processing, biomedical signal processing, array signal processing etc.	Create
CO3	Design digital filters to suit specific requirements for specific applications	Create

List of Experiments / Lab Activities

List of Experiments:

Experiments using MATLAB :

1. Generation and analysis of different signals in time and frequency domains.
2. Study and applications of different transforms
3. Design of Digital Filter: IIR, FIR.
4. Design of multi rate signal system
5. Introduction to DSK 6713 kit and CCS environment
6. Study of input/output, architecture of C6x processor
7. Digital filter design using DSK 6713
8. Implementation of DSP applications using DSK 6713

Text Books

1	Sanjit K. Mitra, “Digital Signal Processing – A Computer based approach”, Tata McGraw-Hill, 4th Edition , 2013
2	Bernard Widrow, Samuel D. Stearns “Adaptive Signal Processing,”, Prentice-Hall, Englewood Cli, NJ, 1985
3	
References	
1	J. G. Proakis, Dimitris K Manolakis, “Advanced Digital Signal Processing Principals, Algorithms and Applications,”, Pearson,2007
2	User manual of TMS320C6713
3	
Useful Links	
1	
2	
3	
4	

CO-PO Mapping															
	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6									
CO1			2												
CO2				2											
CO3						2									
1:Low, 2:Medium, 3:High															

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year B. Tech., Sem. I
Course Code	7EN552
Course Name	Embedded System Design Laboratory
Desired Requisites:	Microcontroller based subjects

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	-	30	30	40	100
		Credits: 1			

Course Objectives

1	To understand the Product Development Process through Mini Project.
2	To understand budgeting through Mini project
3	To use Cortex M3 / M4 processor architecture and its features
4	To learn ARM Cortex –M Architecture and Programming

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**apply** programming skills to integrate hardware peripherals of ARM microcontroller.	Apply
CO2	**test** and **debug** programs for ARM microcontroller.	Analyze
CO3	**develop** and **demonstrate** small embedded systems using ARM C programming and	Create

List of Experiments / Lab Activities/Topics

List of Lab Activities:

1. Experiment 1: Introduction of the development tools and kit
2. Experiment 2: Simple assembly language, embedded C program and study of startup.s file
3. Experiment 3: GPIO Programming and External Peripheral Interfaces
4. Experiment 4: PLL / MAM Programming
5. Experiment 5: Interrupt programming (IRQ and NV-IRQ)
6. Experiment 6: FIQ programming and comparison of FIQ with VIRQ and NVIRQ
7. Experiment 7: Programming Timer to develop applications
8. Experiment 8: Programming Timer to perform capture operation and match facility of timer
9. Experiment 9: Programming PWM and application of it
10. Experiment 10: Programming ADC and DAC
11. Experiment 11: Programming UART
12. Experiment 12: case study of advanced communication protocols
13. Experiment 13: Study of complex algorithm implementation for application development
14. Mini-Project

Textbooks

1	Joseph Yiu, "The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors", Newnes; 3rd edition.
2	Frank Vahid and Tony Givargis, "Embedded System Design", Wiley.
3	Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", E-Man Press LLC.
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2	https://in.coursera.org/
3	https://www.nxp.com/
4	https://www.arm.com/

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3				2									2
CO2		3												2
CO3			3									3		2
1: Low, 2: Medium, 3: High														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli
(Government Aided Autonomous Institute)

AY 2023-24

Course Information

Programme	M. Tech. (Electronics engineering)
Class, Semester	First Year M. Tech., Sem.-I
Course Code	7EN553
Course Name	Digital VLSI Design Lab
Desired Requisites:	Digital Techniques

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/week	**ISE**	**MSE**	**ESE**	**Total**
Interaction	-	30	30	40	100
		Credits: 1			

Course Objectives

1	Demonstrate the use of EDA tools for designing digital circuits
2	Demonstrate Cadence flow (Schematic entry to simulation) for implementing CMOS digital circuits
3	Prepare the students for executing an individual or group problem of medium complexity
4	To explain the relevance of CMOS technology in implementing digital circuits

Course Outcomes (CO) with Bloom's Taxonomy Level

After the completion of the course the student should be able to

CO1	Design and Simulate MOSFET circuits using Cadence tools	Illustrate
CO2	Design and Simulate CMOS circuits using Cadence tools	Develop
CO3	Formulate a research a problem, design, build and simulate either a researched problem or assigned by the supervisor in Digital VLSI Design area independently.	Create

List of Experiments / Lab Activities

A: Using cadence Design Tools:

1. NMOS and PMOS characterization
2. Implementation of CMOS inverter and its characterization for VTC and power
3. Implementation of 2-inpout NAND and NOR. Finding out rise time, fall time of the output and propagation.
4. Implementation of 1-bit full adder using carry-out of the stage to drive the sum output (28 transistor implementation)
5. Implementation of 2-input NAND and NOR gates using different logic styles and compare the performance parameters with complementary CMOS logic style a. Pseudo logic style b. Pass Transistor logic style c. Transmission gate logic style d. Differential cascade voltage switch logic e. Dynamic (pre-charge and evaluate) logic style
6. Implementation of transmission gate based full adder circuit
7. Implementation of four bit Manchester carry chain
8. Implementation of 4-bit barrel shifter using pass transistors

B: Task/mini-project/research problem: For the last lab session which students will have to carry out a task for a period of at least six weeks it is recommended that: 1. Student can search or teacher can assign a course related medium complexity task to a group of student not exceeding two by defining the problem statement suitably.

Text Books	
1	Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits, A System Perspective*", Pearson Education, Second Edition, First Indian Reprint, 2003.
2	Neil Weste, Kamran Eshraghian "*Principles of CMOS VLSI Design*", Addison Wesley/Pearson Education, 2010
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1	Kamran Eshraghian, Pucknell and Eshraghian "*Essentials of VLSI Circuits and Systems*", , Prentice-Hall (India), 2008
2	Sung-Mo Kang, Yusuf Leblebici "*CMOS Digital Integrated Circuits: Analysis and Design*", McGraw Hill Education (India), Third Edition, 2003
3	Neil Weste, David Harris, Ayan Banerjee "*CMOS VLSI Design*", Pearson Education, 2008
Useful Links	
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CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	
CO1				2											
CO2						1									
CO3						1									
CO4			2												

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing (min 40 %), LA1+LA2 should be min 40%

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

Walchand College of Engineering, Sangli *(Government Aided Autonomous Institute)*					
AY 2023-24					
Course Information					
Programme	M.Tech. (Electronics Engineering)				
Class, Semester	First Year M.Tech., Sem I				
Course Code	7EN511				
Course Name	Professional Elective 1-Embedded Linux Programming				
Desired Requisites:	Nil				
Teaching Scheme	**Examination Scheme (Marks)**				
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives	
1	To make students familiar with installation and use of the embedded Linux operating system
2	To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware
3	To give exposure to system design using embedded Linux as per the industry trends

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Apply the understanding of Linux OS for Linux administration	Apply
CO2	Write, compile, debug multi-file, multi-threaded programs under Linux using utilities like make, gdb etc.	Evaluate
CO3	Write programs for peripherals such as GPIO/Keyboard/ Serial port using EL board such as Raspberry pi	Apply

Module	**Module Contents**	**Hours**
I	**Introduction** Introduction to Linux, Linux Distributions, Open source Software, GPL, Facilities in Embedded Linux Boards used in Industry/Market, Important Accessories of Linux boards available/used in industry, Care to take in handling the Linux boards, Development Setup for EL, OS installation, init process, initrd, boot loaders, lilo and GRUB boot loaders, Case studies of Embedded Linux Based Systems.	5
xt Books		

II	**Linux file system and commands** Linux File System, Permissions, CLI and Linux Shells, Linux Commands, Linux concepts, Shell Script, Basic Linux system administration tasks on the RPi. Linux commands for file and process management. Linux Programming, Multi-file C programming Using make utility, Makefile, GNU debugger. Transferring Files Between Systems**,** Kernel, building kernel image	7
III	**Multithreading and Hardware Access** Threads and processes, Multithreaded C programming. EL hardware design issues, Logic-level translation circuitry. Case studies of hardware of frequently used interfaces, Communication with EL board through network, EL GPIO control using sysfs, wiringPi and python. Python libraries	7
IV	**Hardware Interfacing and Programming-I** Using onboard I2C, SPI, and UART capabilities. Circuits to the RPi that interface to its I2C bus, Linux I2C-tools. Communicate between UART devices using both Linux tools and custom C or Python code. Interface to sensors using a serial communication protocol.	7
V	**Hardware Interfacing and Programming-II** Using Interrupt functionality on devices. Increasing the number of available serial UART devices on the RPi using low-cost USB-to-TTL devices. USB Bluetooth adapter for the RPi and connect to it from a mobile device for the purpose of building a basic remote-control application. Using Wi-Fi and Xigbee along with EL board.	7
VI	**Basic Image Processing on Embedded Linux** Camera interfacing to EL board, Capture image and video using OpenCV to perform basic image processing on the RPi. Use OpenCV to perform a computer vision face-detection task.	6

1	Christopher Hallinan, *"Embedded Linux Primer: A Practical Real-World Approach",* Prentice Hall; 1st edition (September 28, 2006), ISBN 978-0137017836
2	Richard Stones, Neil Matthew, *"Beginning Linux Programming"*, Wiley; Fourth edition (2008)
3	Felix Alvaro, "LINUX: Easy Linux For Beginners", Amazon.com
References	
1	P. Raghavan, Amol Lad, Sriram Neelakandan, *"Embedded Linux System Design and Development",* Auerbach Publications; 1 edition (December 21, 2005), ISBN: 978-0849340581 http://crashcourse.ca/introduction-Linux-kernel-programming-2nd-edition
2	Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, Philippe Gerum, "Building Embedded Linux Systems", O'Reilly Media; Second Edition (August 22, 2008) ISBN: 978-0596529680
Useful Links	
1	

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1			2											
CO2				2										
CO3						2								

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE, ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment canbe field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information	
Programme	M.Tech. Electronics Engineering
Class, Semester	First Year M. Tech., Sem. I
Course Code	7EN512
Course Name	Optical Communication
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	- Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	Understand the basics of signal propagation through optical fibers, fiber impairments, components and devices.
2	Classify the various sources and detector for Optical link budget
3	Interpret various types of amplifier used in the optical link.
4	Understand the system performance for long link communication.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Demonstrate the basic elements of optical fiber transmission link, fiber modes configurations and structures.	II
CO2	Identify the different kind of losses, signal distortion in optical wave guides and other signal Degradation factors. Design optimization of SM fibers, RI profile and cut-off wave length	III
CO3	Classify fiber slicing and connectors, noise effects on system performance, operational principles WDM and solutions	IV
CO4	Choose the various optical source materials, LED structures, quantum efficiency, Laser diodes and different fiber amplifiers, optical receivers such as PIN APD diodes, noise performance in photo detector, receiver operation and configuration	V

Module	**Module Contents**	**Hours**
I	**INTRODUCTION** **9** Introduction**,** Ray theory transmission, Total internal reflection, Acceptance angle, Numerical aperture, Skew rays, Electromagnetic mode theory of optical propagation, EM waves, modes in Planar guide, phase and group velocity, cylindrical fibers, SM fibers.	7
II	**TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS** **9** Attenuation, Material absorption losses in silica glass fibers, Linear and Nonl inear Scattering losses, Fiber Bend losses, Midband and farband infra red transmission, Intra and inter Modal Dispersion, Over all Fiber Dispersion, Polarization, non linear Phenomena. Optical fiber connectors**,** Fiber alignment and Joint Losses, Fiber Splices, Fiber connectors, Expanded Beam Connectors	7

III	**SOURCES AND DETECTORS** **9** Optical Sources **:** Semiconductor Physics background, Light emitting diode (LEDs)- structures, materials, Figure of merits, characteristics & Modulation. Laser Diodes -Modes & threshold conditions, Diode Rate equations, resonant frequencies, structures, characteristics and figure of merits, single mode lasers, Modulation of laser diodes, Spectral width , temperature effects, and Light source linearity. Optical Detectors: PIN Photo detectors, Avalanche photo diodes, construction, characteristics and properties, Comparison of performance, Photo detector noise -Noise sources , Signal to Noise ratio , Detector response time	7
IV	**Power Launching and Coupling:** Source to fiber power launching, Lensing schemes, fiber-to-fiber joints, LED coupling to single mode fibers, fiber splicing, Optical fiber connectors. Optical Receiver operation, Preamplifier types, receiver performance and sensitivity, Eye diagrams, Coherent detection, Specification of receivers	6
V	**Optical Transmission System** **Transmission Systems :** Point –to-point link –system considerations, Link power budget and rise time budget methods for design of optical link, BER calculation Optical Amplifiers : Semiconductor optical Amplifier, EDFA, Raman Amplifier, Wideband Optical Amplifiers	6
VI	**Measurements and Advances in Optical Fiber Systems** Fiber Attenuation measurements- Dispersion measurements – Fiber Refractive index profile measurements – Fiber cut- off Wave length Measurements – Fiber Numerical Aperture Measurements – Fiber diameter measurements Principles of WDM, DWDM, Telecommunications & broadband application, SONET/SDH, MUX, Analog & Digital broadband, optical switching	6

Textbooks	
1	Optical Fiber Communications, Keiser, G., ISBN - 9780071164689, by McGraw-Hill, 5th Edition, 2000.
2	Optical Fiber Communications: Principles and Practice, John M. Senior, M. Yousif Jamro, ISBN - 9780130326812, Prentice Hall Internacional series in optoelectronics, 2009
3	
4	

References	
1	Optical Fiber Communications: Principles and Applications, Singal, T.L. ISBN - 9781316870532, 2017, Cambridge University Press
2	Understanding Optical Fiber Communications, Rogers, A.J., ISBN - 9780890064788, Artech House optoelectronics library, 2001
3	
4	

Useful Links	
1	https://archive.nptel.ac.in/courses/108/106/108106167/
2	
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1	3													
CO2				3										
CO3				3										

CO4				3										

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. I
Course Code	7EN513
Course Name	Mobile Communication
Desired Requisites:	Probability Theory and statistics, Digital Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE2**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To introduce the concepts and techniques associated with Wireless Cellular Communication systems.
2	To familiarize with state of art standards used in wireless cellular systems.
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Apply fundamentals of cellular system design to improve performance of cellular network	Apply
CO2	Distinguish between different multiple access technology	Analyze
CO3	Study evolution of mobile communication generation standards	Analyze
CO4	Analyze the different internetworking challenges to provide solutions in wireless mobile networks.	Analyze

Module	**Module Contents**	**Hours**
I	**The Cellular Concept – System Design Fundamentals** Introduction of Cells, Channel Reuse, SIR Calculations, Traffic Handling Capacity: Erlang Performance, Cellular system design, Co channel interference ratio, Co channel interference reduction techniques and methods to improve cell coverage, Frequency management and channel assignment, concepts of cell splitting, handover in cellular system.	8
II	**Multiple Access Technologies** Frequency Division Multiple access (FDMA), Time Division Multiple access (TDMA), Code Division Multiple access (CDMA), spectral efficiency calculations, comparison of T/F/CDMA technologies based on their signal separation techniques, advantages, disadvantages and application areas.	4
III	**GSM Architecture and Interfaces** Introduction to GSM subsystems, GSM Interfaces, GSM architecture, details of following blocks in GSM (Mobile station, Base station systems, Switching subsystems, Home location registers, Visiting location registers, Equipment identity register, Echo canceller), Mapping of GSM layers onto OSI layers, GSM Logical Channels, Data Encryption in GSM, Mobility Management, Call Flows in GSM. Mobile Management: Handoff, Location and Paging, Evolution of mobile technologies 1G to 4G.	8

IV	**Overview of 5G technology** An Overview of 5G requirements, Regulations for 5G, Spectrum Analysis and Sharing for 5G, Channel modeling requirements, Basic requirements of transmission over 5G, Modulation Techniques – Orthogonal frequency division multiplexing (OFDM), generalized frequency division multiplexing (GFDM),	4
V	**Mobile Ad-hoc Network (MANET)** Introduction, properties, applications, architecture, routing in MANET, proactive and reactive routing protocols, hybrid protocol	8
VI	**Mobile Security** Introduction, security in wireless network, information security, security techniques and algorithms, Security protocols.	7

Text Books	
1	T.S.Rappaport*, "Wireless Communications Principles and Practice"*, II Ed. PHI, Publications, 1995
2	Prashant Kumar Patra, Sanjit Kumar Dash, "*Mobile Computing*", 2nd Edition, Scitech, 2014
3	V.K.Garg, J.E.Wilkes, "*Principle and Application of GSM*" Pearson Education, 1999.
4	

References	
1	William C. Y. Lee, *"Mobile Communication Engineering: Theory and Applications"*,2nd Edition, McGraw Hill Publication, 1997
2	Mischa Schwartz, "*Mobile Wireless Communication*", 1st Edition, Cambridge University Press, 2009.
3	

Useful Links	
1	
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CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1		2												
CO2			2											
CO3		2												
CO4			1											

Assessment

The assessment is based on 2 in-semester evaluations (ISE) of 10 marks each, 1 mid-sem examination (MSE) of 30 marks and 1 end-sem examination (ESE) of 50 marks.
MSE is based on the modules taught till MSE (typically Module 1-3) and ESE is based on all modules with 30-40% weightage on modules before MSE and 60-70% weightage on modules after MSE.

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AY 2023-24

Course Information

Programme	M.Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. I
Course Code	7EN514
Course Name	Professional Elective II - System on Chip
Desired Requisites:	Embedded System Design, FPGA Based System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives

1	To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
2	To differentiate embedded system design and system on chip architectures.
3	To motivate students to learn implementation of SOC using MicroBlaze.
4	To teach students to develop IP based system design

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**understand** about SOC design methodology	Understand
CO2	**discuss** the functional and non-functional performance of the system early in the design process to support design decisions	Understand
CO3	**apply** concepts of System on Chip Design methodology for Logic and Analog Cores	Apply
CO4	**analyze** hardware/software trade-offs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.	Analyze

Module	**Module Contents**	**Hours**
I	**Introduction to the System Approach** Concept of system, importance of system architectures, introduction to SIMD, SSID, MIMD and MISD architectures, concept of pipelining and parallelism. Designing microprocessor /Microcontroller based system and embedded system	5
II	**Introduction to SOC** Components of SOC, Design flow of SOC, Hardware/Software nature of SOC, Design Trade-offs, SOC Applications, Differences between Embedded systems and SOCs. System design issues in SOCs.	7
III	**Interconnection** On-chip Buses: basic architecture, topologies, arbitration and protocols, Introduction to AMBA bus, IBM's core connect bus, concept of PLB-processor local bus and on chip peripheral bus (OPB), implementing arbiters in design.	7
IV	**Processors** Concept of Soft embedded processors, Hard vs. Soft embedded processors, Study of Microblaze RISC processor, Programming steps in MicroBlaze Processor.	7
V	**IP based system design** Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP, Technical concerns on IP reuse, IP integration, IP evaluation on FPGA prototypes.	7
VI	**Application Studies/ Case Studies** SOC system design example with Peripherals like USB, UART, Ethernet Etc. using latest FPGA. (Xilinx/ Altera tools) Eclipse IDE development tool for a full SOC system design with embedded C/C++ applications (Xilinx / Altera tools)	6

Textbooks	
1	René Beuchat, Florian Depraz, Andrea Guerrieri, Sahand Kashani, “Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers”, ARM Education Media.
2	Michael J. Flynn and Wayne Luk, “Computer System Design System-on-Chip”, Wiley India Pvt. Ltd.
3	Steve Furber, “ARM System on Chip Architecture “, 2nd Edition, 2000, Addison Wesley Professional.
4	“A Hands-On Guide to Effective Embedded System Design”, XILINX
References	
1	Ricardo Reis, “Design of System on a Chip: Devices and Components”, 1st Edition, 2004, Springer
2	Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3	Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification – Methodologies and Techniques”, 2001, Kluwer Academic Publishers.
4	“Embedded Processor Hardware Design” UG940 (v 2013.2) February 7, 2014
Useful Links	
1	https://www.arm.com/resources/education
2	https://www.xilinx.com/
3	https://swayam.gov.in/nc_details/NPTEL
4	https://www.coursera.org/

CO-PO Mapping														
	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1	2													
CO2	2													
CO3		2			2									
CO4			2											
1: Low, 2: Medium, 3: High														

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher’s assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	M.Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem II
Course Code	7EN521
Course Name	Advanced Embedded Programming
Desired Requisites:	Courses with C programming, Microcontroller, Peripherals and interfacing, Embedded system design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To explain/illustrate/demonstrate need of RTOS and services provided by it.
2	To explain/illustrate/demonstrate services provided by RTOS and their usage
3	To explain/illustrate/demonstrate the internals of RTOS related to TCB.
4	To explain/illustrate/demonstrate how to design of applications using RTOS.(uCOS-II)

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Apply** the knowledge of RTOS to decide whether a given system is suitable for RTOS based implementation and **apply** the theory of task, time, event, memory management, inter-task communication, for solving given situational problems.	Apply
CO2	**Analyse** the given program/ problem/ situation by applying the knowledge acquired.	Analyse
CO3	**Evaluate** the given program or situation and suggest the solution or a better approach, or identify more correct program etc.	Evaluate
CO4	**Design** the tasks and their interactions by using appropriate RTOS services for writing application programs for a given multitasking based (RTOS based) embedded system.	Create

Module	**Module Contents**	**Hours**
I	**Real-time systems contents** Foreground/Background Systems, Pre-emptive and Non-Pre-emptive Kernels, Priority inversion, Deadlock	6
II	**Task management in RTOS** Task structure, RTOS initialization, Task stack, Task states and task state transitions. Creating and deleting a task, Task priority, Case studies of task-based applications	7
III	**Time and Event management in RTOS** Clock tick, delaying a task, resuming the delayed task, getting system time, case study of application based on time management	6
IV	**Case study of Task and Time Management** Case study of application based on task and time management, Internals of RTOS for managing tasks.	7
V	**Intertask Communication in RTOS** Need of Intertask communication, Semaphore, Mailbox, Queues in RTOS. Internals of RTOS for managing tasks and Intertask communication.	6
VI	**Case study of inter-task Communication** Case study of application with inter-task communication, Memory Management in RTOS application.	5

Textbooks	
1	*"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
2	*"Real-Time Concepts for Embedded Systems,"* Qing Li, Caroline Yao Elsevier ISBN: 978-1578201242
3	*"Simple Real-time Operating System: A Kernel,"* Chowdary Venkateswara Amazon, ISBN: 978-1425117825
4	https://freertos.org/Documentation/161204_Mastering_the_FreeRTOS_Real_Time_Kernel-A_Hands-On_Tutorial_Guide.pdf
References	
1	www.micrium.com for uCOS-II related documents, tutorials, downloads.
2	www.nxp.com for processor specific documents.
3	www.wikipedia.org for general OS related basic literature.
4	www.NPTEL.org for OS and RTOS related video courses.
Useful Links	
1	http://downloads.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/tirtos/index.html
2	https://www.youtube.com/watch?v=F321087yYy4
3	https://bit.ly/3nSz3B0 (Texas Instruments RTOS user guide)
4	https://www.segger.com/products/rtos/embos/

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1	3													
CO2	2													
CO3		3												
CO4			3											

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information

Programme	M.Tech. (Electronics Engineering)
Class, Semester	First Year M.Tech., Sem II
Course Code	7EN522
Course Name	Sensor Network and Cloud Computing
Desired Requisites:	TCP-IP Protocols

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives

1	To explain the Wireless Sensor Network and its applications
2	To develop understanding of the Sensor node architecture
3	To understand WSN connectivity with Internet
4	To compare various MAC protocols for Wireless Sensor Network
5	To explain in a concise manner how the general Internet as well as Internet of Things work.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Identify** various challenges and applications of Wireless Sensor Network	Apply
CO2	**Develop** knowledge about Wireless Sensor Network Architecture	Apply
CO3	**Investigate** various MAC protocols for Wireless Sensor Networks	Analyze
CO4	**Explore** and learn about Internet of Things and Cloud	Apply

Module	**Module Contents**	**Hours**
I	**Module 1 : Introduction of WSN** Overview of Wireless Sensor Networks, Applications and Challenges, Mobile ad hoc networks and wireless sensor networks	7
II	**Module 2 Wireless Sensor Node Architecture** Hardware components, Energy consumption , Operating systems and execution environments , examples of sensor nodes	6
III	**Module 3 Wireless Sensor Network Architecture** Types of sources and sinks, Optimization Goals and Figures of Merit, Design principles for WSNs, Gateway Concepts, Need for gateway, WSN and Internet Communication, WSN Tunneling	7
IV	**Module:4 WSN (Medium access control)** Fundamentals of MAC protocols - Low duty cycle protocols and wakeup concepts, Contention Based protocols, Schedule-based protocols - SMAC – BMAC, Traffic-adaptive medium access protocol (TRAMA), The IEEE 802.15.4 MAC protocol.	6

V	**Module 5 IoT** IoT definitions: overview, applications, potential & challenges, and architecture. M2M Protocols for Sensor Networks. IoT CASE Study.	6
VI	**Module 6 Cloud and SDN** Introduction to Cloud Computing including benefits, challenges, and risks Cloud Computing Models. SDN: Introduce software defined networking: the background, the development, and the challenges.	6

Text Books	
1	Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology Protocols and Applications", John Wiley & Sons Inc. Publication ,2007
2	"Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
References	
1	Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks: Architectures and Protocols" ,CRC Press, August 2003
2	Akyildiz, Mehmet Can Vuran**,"**Wireless Sensor Networks" ,John Wiley & Sons Ltd. 2010
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud" Pearson Education
Useful Links	
1	https://nptel.ac.in/noc/courses/noc18/SEM1/noc18-cs09/
2	https://onlinecourses.nptel.ac.in/noc21_cs17/preview

CO-PO Mapping

	Programme Outcomes (PO)														
	1	2	3	4	5	6									
CO1			2	3											
CO2				1		3									
CO3			3			2									
CO4				2		2									

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. II
Course Code	7EN523
Course Name	Automotive Electronics
Desired Requisites:	-

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	- Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To learn the basic control system and sensor required Engine control
2	To learn basic of signal conversion circuit in Automotive system
3	To enhance skill of communication in automotive vehicle
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Use various sensor system to control engine and its devices	III
CO2	Apply knowledge of communication to device for controlling devices	III
CO3	Analyse a problem and identify the computing requirements for engine control instrumentation	IV
CO4		

Module	**Module Contents**	**Hours**
I	**Module 1: The Basics of Electronic Engine Control** Motivation for Electronic Engine Control. Exhaust Emissions, Fuel Economy, Federal Government Test Procedures, Concept of an Electronic Engine Control System, Definition of Engine Performance Terms, Exhaust Catalytic Converters, Electronic Fuel Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition	6
II	**Module 2: Sensors and Actuators** Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensors, Typical Coolant Sensor, Sensors for Feedback Control, Knock Sensors, Angular Rate Sensor, LIDAR, Digital Video Camera, Flex-Fuel Sensor, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Stepper Motors, Ignition System	7
III	**Module 3: Digital Powertrain Control Systems** Digital Engine Control, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Turbocharging, Direct Fuel Injection, Flex Fuel, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes	7
IV	**Module 4: Vehicle Motion Controls** Representative Cruise Control System, Cruise Control Electronics, Antilock Braking System, Electronic Suspension System, Electronic Suspension Control System, Four-Wheel Steering CAR	7

V	**Module 5: Automotive Instrumentation** Modern Automotive Instrumentation, Input and Output Signal Conversion, Display Devices, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement,	6
VI	**Module 6: Vehicle Communications** IVN, CAN, Local Interconnect Network (LIN), FlexRay IVN, MOST IVN, Vehicle to Infrastructure Communication, Vehicle-to-Cellular Infrastructure, Short-Range Wireless Communications, Satellite Vehicle Communication, GPS Navigation, Safety Aspects of Vehicle-to-Infrastructure Communication	6

Textbooks	
1	*Understanding Automotive Electronics An Engineering Perspective by* William Ribbens, Elsevier
2	Bosch Automotive Electrics and Automotive Electronics: Systems and Components, Networking and Hybrid Drive, Robert Bosch GmbH, Springer Science & Business Media, 2013
3	
4	

References	
1	Automotive Electronics Design Fundamentals, Najamuz Zaman, Springer Cham, October 2016
2	Automotive Electronics Handbook, Ronald K. Jurgen, McGraw Hill Professional, 1999
3	
4	

Useful Links	
1	
2	
3	

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1				3										
CO2				3										
CO3				3										
CO4														

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. II
Course Code	7EN571
Course Name	Advanced Embedded Programming Lab
Desired Requisites:	Theory/Lab Courses with C programming, Microcontroller Peripherals and Interfacing, Embedded System Design.

Teaching Scheme		Examination Scheme (Marks)			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	- Hrs/ Week	30	30	40	100
		Credits: 1			

Course Objectives	
1	To learn system Architecture, configuration and Programming for Embedded Linux Based System.
2	To facilitate students to gain practical experience of RTOS and services provided by it.
3	To help students to co-relate the RTOS theory with the RTOS implementation.
4	To provide exposure to industry applications and facilitate for writing applications using Linux and RTOS.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Installation of OS Process and write programs / scripts for Embedded Linux Board.	Apply
CO2	Verify the RTOS fundamentals, through illustrative programs and demonstrate usage of task, time, and event management, Intertask communication using a simulator. (Programming skill, Modern Tools)	Analyze
CO3	Implement a given logic as an RTOS based application. Create document of the same and demonstrate using simulation tools. (Programming skill, Independent and teamwork, Modern Tools)	Create

List of Experiments / Lab Activities/Topics

List of Topics(Applicable for Interaction mode):

List of Lab Activities:

1. Experiments to revise an Embedded System Design
2. Experiment to study Linux distribution installation, configuration and basic commands of it.
3. Experiment to study configuration for an Embedded Linux Board.
4. Experiment to access GPIO of an Embedded Linux Board to control components / devices interfaced to it.
5. Demonstration of RTOS based application in keil micro vision
6. Writing of RTOS based application .
7. Finding the type of kernel for a given RTOS (Pre-emptive or Non-pre-emptive)
8. Semaphore for managing shared resource and task synchronization
9. Demonstration of Clock tick and its effect of event timing in RTOS based systems.
10. Semaphore for event synchronization
11. Using mailbox facility in RTOS
12. Using queue facility in RTOS
13. Avoiding deadlock in RTOS

Textbooks	
1	"Mastering Embedded Linux Programming", Second Edition, Chris Simmonds.

2	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux" first Edition, Derek Molloy
3	*"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
4	*RTOS Lab Manual*
References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	www.micrium.com for uCOS-II related documents, tutorials, downloads.
3	https://www.freertos.org/Documentation/RTOS_book.html
4	Everything You Need to Know about RTOS (pdf book) by Silabs
Useful Links	
1	https://www.linux.org/
2	https://www.raspberrypi.org/
3	www.highintegritysystems.com/rtos for RTOS tutorials
4	https://www.youtube.com/watch?v=ECEvUEkSSLg for videos by Renesas Inc.

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1		3												
CO2			3											
CO3				2										

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

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AY 2023-24

Course Information

Programme	M.Tech. (Electronics Engineering)
Class, Semester	First Year M.Tech., Sem II
Course Code	7EN545
Course Name	Mini Project -Sensor Networks and Cloud Computing
Desired Requisites:	None

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/week	Nil			
Interaction	-	**Credits: 1**			

Course Objectives

1	To understand the Product Development Process through Mini Project.
2	To understand budgeting through Mini project
3	To use Wireless Sensor Network protocols
4	To learn IoT sensors interfacing
5	To understand the importance of document design by compiling Technical Report on the Mini Project work carried out.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Identify** various challenges and applications of Wireless Sensor Network	Apply
CO2	**Develop** knowledge about Wireless Sensor Network Architecture	Apply
CO3	**Investigate** various MAC protocols for Wireless Sensor Networks	Analyze
CO4	**Explore** and learn about Internet of Things and Cloud	Apply

Mini Project Guideline

1. The students must understand following aspects while planning Mini Project
   a. Concept of WSN and IoT
   b. Importance
   c. Interdisciplinary
   d. Challenges
   e. Various applications/smart objects
   f. Major Players/Industry, Standards.

2. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare synopsis

3. The progress of work and discussion must be documented.

4. Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty

5. The Student must submit a brief project report(25-30 pages) that must include the following
   a. Introduction
   b. Literature survey
   c. Hardware & Software Requirements
   d. System Design Architecture
   e. Implementation (screenshots to be included)
   f. Testing
   g. Conclusion
   h. Future enhancements.
   j. Bibliography

Text Books	
1	Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology Protocols and Applications", John Wiley & Sons Inc. Publication ,2007
2	"Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
References	
1	Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks: Architectures and Protocols" ,CRC Press, August 2003
2	Akyildiz, Mehmet Can Vuran**,"**Wireless Sensor Networks" ,John Wiley & Sons Ltd. 2010
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud" Pearson Education
Useful Links	
1	https://nptel.ac.in/noc/courses/noc18/SEM1/noc18-cs09/
2	https://onlinecourses.nptel.ac.in/noc21_cs17/preview

CO-PO Mapping															
	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3

CO1			2	3											
CO2				1		3									
CO3			3			2									
CO4				2		2									
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.															

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

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AY 2023-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year B. Tech., Sem. II
Course Code	7EN531
Course Name	Professional Elective 3 - Embedded Linux System Design
Desired Requisites:	Embedded Linux

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives	
1	To facilitate students to learn the web technology on embedded Linux platform.
2	To help the students to design static and dynamic website for solving social problems using embedded Linux and web framework.
3	To help the students to develop embedded Linux based system
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	**Design** a website using a frontend, backend languages/ scripts and framework.	Understand
CO2	**Connect** embedded system with front end / back end using Embedded Linux	Apply
CO3	**Design** and **develop** web based solution for social problems using the Embedded Linux.	Create
CO4	**Implement** solution for social problems using the Embedded Linux.	Create

Module	**Module Contents**	**Hours**
I	**Introduction to web technology** Fundamentals of Web technology, Web server, Web Client, Server and client side scripting. Installation of Web server on EL boards and accessing them over intranet.	4
II	**Web Programming** Frontend design, using HTML and CSS, Backend design using PHP, Python, SQL; Using web server for static / dynamic content, Responsive site basics and design.	8
III	**Web Design Framework** PHP Frameworks Code igniter / Python Frameworks Flask, Basics of database and updating database directly from Embedded Linux based system, dynamic webpage for web based system.	8
IV	**System Configuration** Configure Network Setup & Remote access, Controlling GPIOs, Installing required packages / libraries, Interfacing various peripherals, Sensors, Camera etc. to Embedded Linux Board, accessing / handling hardware using Python.	8
V	**System Design** Design steps to implement system using Embedded Linux platform, Web based system design for real world problem, Introduction to device driver, architecture, types of it and programming example.	8
VI	**Applications** Case study on embedded Linux system design for web based Applications, IoT Applications, Image Processing based Applications.	4

Textbooks	
1	Robin Nixon, Learning PHP, MySQL & JavaScript, O'Reilly publication, 4th Edition, 2015,ISBN: 9789352130153
2	Kogent Learning Solutions Inc, Web Technologies: HTML, JAVASCRIPT, PHP, Dreamtech Press(2009) ISBN: 978-8177229974
3	Carlos de la Guardia , "Python Web Framework", O'Reilly Media, Inc.
4	John Madieu, "Linux Device Drivers Development", Ed. 1 2017, ISBN: 9781785280009
References	
1	Frank Vasquez, Chris Simmonds, "Mastering Embedded Linux Programming: Create fast and reliable embedded solutions with Linux 5.4 and the Yocto Project 3.1", 3rd edition, Packt Publishing.
2	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux", 1st edition, Wiley.
3	Fabrizio Romano, Gaston C. Hillar, Arun Ravindran "Learn Web Development with Python: Get hands-on with Python Programming and Django web development", Packt Publishing Limited.
Useful Links	
1	https://www.edx.org/
2	https://www.udacity.com/
3	https://www.coursera.org/
4	https://www.kernel.org/
5	https://www.raspberrypi.org/

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													
CO2	2													
CO3		2			2									
CO4			2											2
1: Low, 2: Medium, 3: High														

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information

Programme	MTech. (Electronics Engineering)
Class, Semester	First Year MTech., Sem II
Course Code	7EN532
Course Name	Professional Elective 3-Biomedical Signal Processing
Desired Requisites:	Signals and Systems, Digital Signal Processing

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	60	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives

1	To study origins and characteristics of some of the most commonly used biomedical signals including ECG, EEG, evoked potentials, and EMG
2	To explore application of established engineering methods to complex biomedical signals problems

Course Outcomes (CO) with Bloom's Taxonomy Level

After the completion of the course the student should be able to

CO1	Apply signal processing techniques to biomedical signals	Apply
CO2	Analyze ECG and EEG signal with characteristic feature points	Analyz
CO3	Model a biomedical system	Create

Module	**Module Contents**	**Hours**
I	**Introduction to Biomedical Signals** Introduction to Biomedical Signals, The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis, Signal Conversion Systems, Conversion requirements for biomedical signals, Signal conversion circuits. Application areas of Bio -Signal analysis – EEG, ECG, Phonocardiogram, Spiro Gram, Evoked Signals	6
II	**Signal Averaging and Data Compression Techniques** Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding	6
III	**Adaptive Noise Cancellation** Adaptive interference / Noise cancellation: Types of noise in biosignals; Digital filters - IIR and FIR - Notch filters - Optimal and adaptive filters. Weiner filters - steepest descent algorithm - LMS adaptive algorithm - Adaptive noise canceller - cancellation of 50 Hz signal in ECG - Cancellation of maternal ECG in foetal electrocardiography	6

IV	**Cardiological signal processing** Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor.	7
V	**Neurological signal processing** Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection	6
VI	**Modeling of Biomedical Systems** Motor unit firing pattern, Cardiac rhythm, Formants and pitch of speech, Point process, Parametric system modeling, Autoregressive model, Autocorrelation method, Application to random signals, Computation of model parameters, Levinson-Durbin algorithm, Computation of gain factor, Covariance method, Spectral matching and parameterization, Model order selection, Relation between AR and Cepstral coefficients	8

Text Books	
1	Reddy D C. "Modern Biomedical Signal Processing – Principles and Techniques", TMH, New Delhi, 2005
2	Eugene N. Bruce, "Biomedical Signal Processing and Signal Modeling", A Wiley-Interscience Publication JOHN WILEY & SONS, INC

References	
1	1. Akay M. "Biomedical Signal Processing", Academic press, California,1994.
2	Bronzino J D "The Biomedical Engineering handbook", CRC and Free press, Florida, 1995.

Useful Links	
1	NPTEL LECTURES

CO-PO Mapping

	Programme Outcomes (PO)														
	1	2	3	4	5	6									
CO1			2												
CO2				2											
CO3						1									

The strength of mapping is to be written as 1,2,3; Where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 203-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Sem. II
Course Code	7EN533
Course Name	Professional Elective 4- Design and Analysis of Algorithm
Desired Requisites:	Data Structure and Algorithms

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To provide different algorithm approaches like static, dynamic, iterative and recursive techniques.
2	To explain Comparative features of algorithms on the basis of space, time computational complexities,
3	To explain the selection criteria for identifying, formulating and applying a typical algorithm for given problem.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Interpret different algorithm approaches like static, dynamic, iterative and recursive techniques.	Apply
CO2	Compare the different algorithms on the basis of space, time computational complexities	Analyze
CO3	Identify the optimum algorithm for given problem.	Analyze

Module	**Module Contents**	**Hours**
I	**Introduction** Static and dynamic structures, stacks, queues, dynamic memory allocation and pointers, linked stacks and queues, trees and recursion, Hashing:- Sparse-table, hash function, collision resolution with open addressing and collision resolution by chaining	6
II	**Searching and Sorting Algorithms** Sequential search, Binary search, Comparison of trees, Insertion sort, Selection sort (Heap sort), Shell sort. Computational Complexity, lower bound, & comparison of searching and sorting algorithm	6
III	**Divide and Conquer** Merge sort, quick sort (portioning), Matrix multiplication algorithm, Limitation of divide and conquer. Computational complexity of divide and conquer algorithms.	6
IV	**Dynamic Programming & Greedy Approach** Binomial Coefficients, Floyd's algorithm for shortest path, Chain matrix multiplication, optimal binary search trees and the traveling salesperson problem, Dynamic programming approach to 0-1 knapsack problem, Minimum spanning traces algorithms and their Comparison.	8

V	**Back Tracking & Branch and Bound** Back tracking techniques, the n-queens problem, Back tracking algorithm's efficiency using Monte Carlo algorithm. Graph coloring, the Hamiltomnian circuits' problem. Backtracking Algorithm for 0-1 Knapsack problem and its comparison	8
VI	**Theory of NP** The three general categories of problems. The sets P & NP. NP complete problems, NP-Hard, NP-easy, NP – Equivalent problems, NP Hard problems	5

Text Books	
1	*"Fundamentals of Computer Algorithms",* Ellis Horowitz, Sartaj Sahani, Sangutherar Rajasekaran., Galgotia Pubication Ltd, 2010
2	*"Design and Analysis of Algorithms",* I. Chandra Mohan, PHI Publication, 2012.
3	*"Analysis of Computer Algorithms",* Horowitz and Sahni, Galgotia Publishers., 2007
4	

References	
1	*"Foundation of Algorithms",* Richard E. Neapolita & Kumarss Naimipour (Northeastern Illinois University), D.C. Heath and Company, Publication, 1996.
2	*"Data Structures and Program Design in C",* Robert L. Kruse & Brunce P. Leung et. Al, PHI Publication, 1984.
3	*"Introduction to Algorithms" Coremn, Leiserson, Rivest, PHI Publication, 2012.*

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1		1												
CO2	2													
CO3			2											

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	M. Tech. (Electronics Engineering)
Class, Semester	First Year M. Tech., Semester II
Course Code	7EN534
Course Name	Professional Elective 4 Pattern Recognition and Image Analysis
Desired Requisites:	Signal Processing

Teaching Scheme		**Examination Scheme (Marks)**			
ISE2	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
10	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To imparts knowledge in the area of image and image processing
2	To learn the fundamentals of Pattern recognition and to choose an appropriate feature
3	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Use foundational techniques of image processing and analysis such as filtering, segmentation and local features to solve image processing problems of real world application	Apply
CO2	Apply image processing and pattern recognition techniques to detect objects and activities in images	Apply
CO3	Compare and parameterize different learning algorithms.for pattern recognition	Analyze
CO4		

Module	**Module Contents**	
I	**Fundamentals of Image Processing:** Pixel brightness transformation, position dependent brightness correction, gray scale transformation; geometric transformation, local pre-processing image smoothening, edge detectors, zero-crossing, scale in image processing, canny edge detection, parametric edge models, edges in multi spectral images, local pre-processing and adaptive neighbourhood pre-processing; image restoration	**5**
II	**Image Segmentation:** Threshold detection methods, optimal thresholding, multispectral thresholding, thresholding in hierarchical data structures; edge based image segmentation- edge image thresholding, edge relaxation, border tracing, border detection	**3**

III	**Mathematical Morphology:** Basic morphological concepts, four morphological principles, binary dilation, erosion, Hit or miss transformation, opening and closing; thinning and skeleton algorithms; Morphological segmentation –particles segmentation and watersheds, particle segmentation	**5**
IV	**Image Textures:** statistical texture description, methods based on spatial frequencies, co-occurrence matrices, edge frequency, and texture recognition method, applications Image representation and description-representation, boundary descriptors, regional descriptors	**4**
V	**Fundamentals of Pattern Recognition:** Basic concepts of pattern recognition, fundamental problems in pattern recognition system, design concepts and methodologies, example of automatic pattern recognition systems, a simple automatic pattern recognition model	**4**
VI	**Pattern Classification Algorithms:** Pattern classification by distance function: Measures of similarity. Clustering criteria. K means algorithm. Pattern classification by like hood function: Pattern classification as a Statistical decision problem. Bayes classifier for normal patterns	**5**

Text Books	
1	Earl Gose and Richard Johnsonbaugh Steve Jost, "Pattern Recognition and Image Analysis", PHI publication.
2	Sing Tze Bow, M. Dekker, "Pattern Recognition and Image Processing", Springer, 1992
3	

References	
1	Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Addinson – Wesley.
2	M. A. SID – AHMED, "Image Processing Theory Algorithms and Architecture", McGraw Hill Inc.
3	

Useful Links	
1	https://www.coursera.org/
2	
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)													
	1	2	3	4	5	6								
CO1	3													
CO2			2											
CO3						2								
CO4														

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High

Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	M.Tech. (Electronics Engineering)
Class, Semester	First Year M.Tech., Sem II
Course Code	7OE508
Course Name	Open Elective - Introduction to Embedded Systems
Desired Requisites:	None

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-	Nil			
Interaction	-	**Credits: 3**			

Course Objectives

1	To introduce Embedded Systems and their applications
2	To develop understanding about Microcontrollers
3	To introduce hardware components of Embedded Systems
4	To explain fundamentals of Arduino
5	To explore Arduino based applications and programming

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Understand** Embedded Systems and Identify their applications	Apply
CO2	**Develop** knowledge about hardware and software of Embedded Systems	Apply
CO3	**Analyze** Arduino based systems and their programming	Analyze
CO4	**Explore** and learn Arduino based systems applications	Apply

Module	**Module Contents**	**Hours**
I	**Module 1 Introduction** Embedded Systems and general purpose computer systems, history, classifications, applications and purpose of embedded systems Characteristics and Applications of embedded systems: operational and non-operational quality attributes. Embedded Systems Applications-Application specific – washing machine, domain specific - automotive	7
II	**Module 2 Core of embedded systems** Microprocessors and microcontrollers, RISC and CISC controllers, Big endian and Little endian processors, Application specific ICs, Programmable logic devices, COTS, sensors and actuators, communication interface, embedded firmware, other system components.	7

III	**Module 3 Embedded Hardware** Memory map, i/o map, interrupt map, processor family, external peripherals, memory – RAM , ROM, types of RAM and ROM, memory testing, CRC ,Flash memory. **Peripherals:** Control and Status Registers, Device Driver, Timer Driver - Watchdog Timers	7
IV	**Module 4 Introduction to Arduino** Arduino device,Features of Arduino, Components of Arduino board,Description of Microcontrollers, Installation of Arduino IDE on Ubuntu Linux OS Run the arduino executable file, Using IDE to prepare Arduino sketch, Uploading and running the sketch,Program notation: variables, functions, control flow, Arduino conventions.The concept of a program variable.Numerical values and basic numerical operators.if/then/else Iteration using for loops.Real world timing and the delay() function	7
V	**Module 5 Input/Ouput Progrmming** Sensor Inputs:- Definition, Types. Interfacing arduino to different sensors- light sensor, temperature sensor, humidity sensor, pressure sensor sound sensor, distance ranging sensor, water/detector sensor, smoke, gas, alcohol sensor, ultrasonic range finder ,Displays: Basics of LED's and LCD's. Interfacing arduino to LED's- blinking single LED, blinking multiple LED's, 7 segment display , traffic light ,LED flashes ,LED dot matrix ,pulsating lamp. Interfacing to LCD's- Basic LCD control, LCD temperature control, display a message on LCD screen, scrolling of text Touch screens, Reading and writing to SD card	7
VI	**Module 6 Arduino Applications** Case studies : Arduino based robot car , Arduino based PLC, industrial application	4

Text Books	
1	Shibu K V , "Introduction to embedded systems", Tata Mcgraw-Hill, 1st edition
2	"Arduino Cookbook,"Michael Margolis

References	
1	"Embedded Systems", Rajkamal, Tata Mcgraw-Hill
2	"Beginning Arduino", Michal Mc Roberts, Second Edition
3	Michal Mc Roberts "Beginning Arduino" Second Edition, Technology in Action

Useful Links	
1	NPTEL Lectures
2	

CO-PO Mapping															
	Programme Outcomes (PO)														
	1	2	3	4	5	6									
CO1			2												
CO2						3									
CO3			3			2									
CO4				2		2									
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.															

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)