Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2022-23

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN401
Course Name	Power Electronics and Drives
Desired Requisites:	Basic Electrical Engineering, Circuit Theory

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	**Explain** the working of modern power semiconductor devices and their applications.
2	**Explain** the working of power converter circuits like controlled rectifier, inverter, AC voltage controller and chopper and provide the knowledge of performance parameters of converters in the analysis of their performance.
3	**Explain** the use of different power control techniques like converters, choppers, inverters and cycloconverters to control the speed of DC motors and Induction motors.
4	**Illustrate** to choose an appropriate power electronic circuit and a power semiconductor device while designing an electrical power control system.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Explain** the working of power semiconductor devices such as SCR, GTO, Power MOSFET and IGBT.	Understand
CO2	**Analyze** the performance of controlled rectifiers, DC to DC converters, Inverters, AC to AC converter.	Analyze
CO3	**Evaluate the** performance parameters of controlled rectifier, DC to DC converter, DC to AC converter and AC to AC converter.	Evaluate
CO4	**Analyze** the speed control techniques/ methods for AC and DC motors.	Analyze

Module	**Module Contents**	**Hours**
I	**Power Semiconductor Devices** SCR (Silicon Controlled Rectifier): two transistor model, protection circuits, series and parallel operation of SCR, triggering and commutation circuits; GTO, TRIAC, DIAC, Power Diode, Power BJT, Power MOSFET, IGBT.	7
II	**Phase Controlled Rectifiers** Single phase half and full wave controlled rectifier with R and RL load, Single phase half controlled (semiconverter) and fully controlled bridge rectifier. Three phase half wave controlled rectifier with resistive load, three phase half controlled and fully controlled bridge rectifier with R and RL load; Calculation of performance parameters of line commutated converters: Fourier analysis; effect of source impedance on the performance of controlled rectifiers.	9
III	**Inverters and AC voltage Controllers** Single phase half and full bridge inverter using transistor/MOSFET/IGBT, performance parameters, Fourier analysis of inverter output voltage; Three phase bridge inverter- 120^0 and 180^0 conduction mode; PWM inverters; Series and Parallel resonant inverter. AC voltage controllers: single phase and three phase AC voltage controllers; cycloconverters: single phase to single phase, three phase to single phase, three phase to three phase cycloconverter.	8
IV	**DC to DC converters** Choppers: principles of operation, control strategies: TRC, current limit control; types of chopper, step up chopper, multiphase chopper; SMPS.	4

V	**D.C. Motor Control** Equivalent circuit, speed torque characteristics (separately excited and series motor), operating modes, single phase and three phase controlled rectifier fed drives; four quadrant drive-single phase and three phase dual converter; Chopper-fed DC drive.	6
VI	**A.C. Motor Control** Equivalent circuit, speed torque characteristics, speed control methods-stator voltage control, rotor voltage control, frequency control, stator voltage and frequency control (V/F); Vector Control.	6

Text Books	
1	M. D. Singh & K. B. Khanchandani, "*Power Electronics*", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
2	M.H. Rashid, "*Power Electronics: Circuits, Devices & Applications*", Third Edition, PHI, New Delhi, 2008.
3	P. S. Bimbhra, "*Power Electronics*", Third Edition, Khanna Publishers, 2004.
4	
References	
1	P. C. Sen, "*Power Electronics*", First Edition, Tata McGraw Hill Publishing Company Ltd, 2008.
2	V. R. Moorthi, "*Power Electronics-Devices, Circuits and Industrial Applications*", Oxford University Press, 2010.
3	Ned Mohan, T. M. Undeland, W. P. Robbins, "*Power electronics-Converters, Applications and Design*", Third Edition, John Wiley and Sons Inc., 2003.
Useful Links	
1	https://nptel.ac.in/courses/108/105/108105066/#
2	https://nptel.ac.in/courses/108/108/108108077/
3	https://nptel.ac.in/courses/108/102/108102145/

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													
CO2	2	3	1											2
CO3	2	3												
CO4		2	2											2

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2022-23

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN402
Course Name	Real Time Operating System
Desired Requisites:	Courses with C programming, Microcontroller, Peripherals and interfacing, Embedded system design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 2**			

Course Objectives

1	To explain/illustrate/demonstrate need of RTOS and services provided by it.
2	To explain/illustrate/demonstrate services provided by RTOS and their usage
3	To explain/illustrate/demonstrate the internals of RTOS related to TCB.
4	To explain/illustrate/demonstrate how to design of applications using RTOS.(uCOS-II)

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Apply** the knowledge of RTOS to decide whether a given system is suitable for RTOS based implementation and **apply** the theory of task, time, event, memory management, inter-task communication, for solving given situational problems.	Apply
CO2	**Analyse** the given program/ problem/ situation by applying the knowledge acquired.	Analyse
CO3	**Evaluate** the given program or situation and suggest the solution or a better approach, or identify more correct program etc.	Evaluate
CO4	**Design** the tasks and their interactions by using appropriate RTOS services for writing application programs for a given multitasking based (RTOS based) embedded system.	Create

Module	**Module Contents**	**Hours**
I	**Real-time systems contents** Foreground/Background Systems, Pre-emptive and Non-Pre-emptive Kernels, Priority inversion, Deadlock	6
II	**Task management in RTOS** Task structure, RTOS initialization, Task stack, Task states and task state transitions. Creating and deleting a task, Task priority, Case studies of task-based applications	4
III	**Time and Event management in RTOS** Clock tick, delaying a task, resuming the delayed task, getting system time, case study of application based on time management	4
IV	**Case study of Task and Time Management** Case study of application based on task and time management, Internals of RTOS for managing tasks.	4
V	**Intertask Communication in RTOS** Need of Intertask communication, Semaphore, Mailbox, Queues in RTOS. Internals of RTOS for managing tasks and Intertask communication.	4
VI	**Case study of inter-task Communication** Case study of application with inter-task communication, Memory Management in RTOS application.	6

Textbooks

1	*"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
2	*"Real-Time Concepts for Embedded Systems,"* Qing Li, Caroline Yao Elsevier ISBN: 978-1578201242
3	*"Simple Real-time Operating System: A Kernel,"* Chowdary Venkateswara Amazon, ISBN: 978-1425117825
4	https://freertos.org/Documentation/161204_Mastering_the_FreeRTOS_Real_Time_Kernel-A_Hands-On_Tutorial_Guide.pdf
References	
1	www.micrium.com for uCOS-II related documents, tutorials, downloads.
2	www.nxp.com for processor specific documents.
3	www.wikipedia.org for general OS related basic literature.
4	www.NPTEL.org for OS and RTOS related video courses.
Useful Links	
1	http://downloads.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/tirtos/index.html
2	https://www.youtube.com/watch?v=F321087yYy4
3	https://bit.ly/3nSz3B0 (Texas Instruments RTOS user guide)
4	https://www.segger.com/products/rtos/embos/

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3												2	
CO2	2												2	
CO3		3											3	
CO4			3											3
The strength of mapping is to be written as 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO.														

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AY 2022-23

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN403
Course Name	Humanities -4 Legal, IPR, Safety
Desired Requisites:	

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	1 Hrs/Week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	15	10	25	50
Practical	-				
Interaction		**Credits: 1**			

Course Objectives

1	To introduce the students about Legal, IPR, Safety laws.
2	To disseminate knowledge on patents, patent regime in India and abroad and registration aspects.
3	To be aware about current trends in IPR and Govt. steps in fostering IPR.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Understand about Indian industry Legal, IPR, Safety laws	Understand
CO2	Interpret patent and copyright in innovative research work.	Apply
CO3	Illustrate the importance of Indian industry Legal, IPR, Safety laws	Analyze
CO4		

Module	**Module Contents**	**Hours**
I	Overview of Bureau of Indian Standards Act of 1986	2
II	The Right to Information Act of 2005, In order to promote public education andpublic safety	2
III	Intellectual Property, Patents, Copyrights, Trademarks,	3
IV	Other forms of IP, Current Contour,	3
V	The Factories Act, 1948, The Mines Act, 1952,	2
VI	The Dock Workers (Safety, Health & Welfare) Act, 1986.	1

Text Books

1	Nithyananda, K V. (2019). Intellectual Property Rights: Protection and Management. India, IN: Cengage Learning India Private Limited.
2	D.S. S. Ganguly and C S Changeriya Labor & Industrial Acts & Laws (Safety Management)
3	
4	
5	

References

1	Ahuja, V K. (2017). Law relating to Intellectual Property Rights. India, IN: Lexis Nexis
2	
3	
4	

Useful Links

1	Cell for IPR Promotion and Management (http://cipam.gov.in/)
2	https://law.resource.org/pub/in/bis/manifest.med.html

3	World Intellectual Property Organization (https://www.wipo.int/about-ip/en/)
4	Office of the Controller General of Patents, Designs & Trademarks (http://www.ipindia.nic.in/)
5	https://labour.gov.in/industrial-safety-health

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1								1					1	1
CO2									2					2
CO3							1						2	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.														

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN451
Course Name	Power Electronics and Drives Lab
Desired Requisites:	Basic Electrical Engineering, Circuit Theory

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	**Explain** the V-I characteristics of power semiconductor devices and their use as a switch.
2	**Demonstrate** the operating and handling procedure (i.e. safety measures) of power electronic experimental set ups.
3	**Explain** the need of isolating power circuit ground and control circuit ground (use of Powerscope or isolation transformer) during observation of waveforms and measurement of input and output voltage of a power electronic circuit i.e. controlled rectifier, inverter and chopper.
4	**Demonstrate** the use of simulation software (PSIM, MATLAB, PSPICE) in the analysis and design of power electronic circuits /systems.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Experiment with** power semiconductor devices and plot its V-I characteristics.	Understand
CO2	**Build** and **test** power electronic circuits (controlled rectifiers, inverters, choppers)	Apply
CO3	**Analyze** the performance power electronic circuits (controlled rectifiers, inverters, choppers)	Analyze
CO4	**Examine** and **compare** speed control techniques/ methods for AC and DC motors.	Analyze

List of Experiments / Lab Activities

The primary objective of this laboratory is to impart the practical knowledge of power electronic circuits for the conversion and control of electrical energy. This laboratory course develops a basic foundation for analysis, design, test, and control of power electronics converters by experimentation and simulation.

List of Experiments: (Minimum 8 experiments)

Study of power semiconductor devices: SCR, Power MOSFET, IGBT.

SCR triggering circuits: R, RC, and UJT

Single phase half controlled bridge rectifier.

Single phase fully controlled bridge rectifier.

Single phase transistorized inverter.

Single phase to Single phase Cycloconverter.

Design and implementation of a Type-A chopper (Power MOSFET based) circuit.

Single/ Three phase controlled rectifier fed DC drive.

Chopper fed DC drive.

Three phase induction motor drive.

Four quadrant DC drive (Dual converter).

Speed control of brushless DC motor.

Simulation of Controlled Rectifier and Three Phase Inverter Circuit using MATLAB/ PSIM.

Text Books

1	M.H. Rashid, "*Power Electronics: Circuits, Devices & Applications*", Third Edition, PHI, New Delhi, 2008.

2	M. D. Singh & K. B. Khanchandani, "*Power Electronics*", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
3	V. R. Moorthi, "*Power Electronics: Devices, Circuits and Industrial Applications*", Oxford University Press, 2010.
4	

References	
1	D. R. Grafham, J. C. Hey, "*SCR Manual*", Fifth Edition, General Electric, New York, 1972.
2	https://www.powersimtech.com/wp-content/uploads/2021/01/PSIM-User-Manual.pdf
3	
4	

Useful Links	
1	https://powersimtech.com/products/psim/capabilities-applications/
2	https://in.mathworks.com/solutions/power-electronics-control/power-electronics-simulation.html
3	https://www.plexim.com/products/plecs
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	1			3										
CO2				3	3									2
CO3		1		3	3									2
CO4	1			3	2									

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN452
Course Name	Real Time Operating System Lab
Desired Requisites:	Theory/Lab Courses with C programming, Microcontroller Peripherals and Interfacing, Embedded System Design.

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2hrs/ week				
Interaction	-	**Credits: 1**			

Course Objectives

1	To facilitate students to gain practical experience of RTOS and services provided by it.
2	To help students to co-relate the RTOS theory with the RTOS implementation.
3	To provide exposure to industry applications and facilitate for writing applications using RTOS.
4	To help students to acquire skills of using modern tools to develop and test RTOS based project.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Apply** the theoretical knowledge and demonstrate the basics of RTOS and the acquired skills of managing RTOS based project. (Practical Experience, Modern Tools)	Apply
CO2	**Prove/Verify** the RTOS fundamentals, through illustrative programs and **demonstrate** usage of task, time, and event management, Intertask communication using a simulator. (Programming skill, Modern Tools)	Apply
CO3	**Analyze** given RTOS based problem by applying the theoretical knowledge acquired. (Problem Solving, Modern Tools)	Analyze
CO4	**Implement** a given logic as an RTOS based application. Create document of the same and demonstrate using simulation tools. (Programming skill, Independent and teamwork, Modern Tools)	Create

List of Experiments / Lab Activities

List of Lab Activities:

Demonstration of RTOS based application and related practices in industry
Writing of RTOS based application for creating given signals on digital I/O
Finding the type of kernel for a given RTOS (Pre-emptive or Non-pre-emptive)
Semaphore for managing shared resource and task synchronization
Assigning Mini-project problems. Demonstration of Clock tick and its effect of event timing in RTOS based systems.
Semaphore for event synchronization
Using mailbox facility in RTOS
Using queue facility in RTOS
Avoiding deadlock in RTOS
Building a small embedded application using an RTOS (Mini-Project) (Solving given problem by writing relevant program, Simulation, documentation, Demonstration, Period is around 3 weeks as a part of Lab ESE. The application will be typically based on consumer/industrial product.)
Arrange guest lecture on VxWorks Operating System.

Textbooks

1	*"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
2	*RTOS Lab Manual*
3	https://www.beningo.com/5-best-practices-for-designing-rtos-based-applications/

4	https://tinyurl.com/nhcw542x (University of Waterloo RTOS book)
References	
1	www.micrium.com for uCOS-II related documents, tutorials, downloads.
2	www.nxp.com for processor specific documents.
3	https://www.freertos.org/Documentation/RTOS_book.html
4	Everything You Need to Know about RTOS (pdf book) by Silabs
Useful Links	
1	www.highintegritysystems.com/rtos for RTOS tutorials
2	https://www.youtube.com/watch?v=ECEvUEkSSLg for videos by Renesas Inc.
3	University of Waterloo lecture material on RTOS
4	Micrium µC/OS-II Documentation (Documentation of RTOS company)

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3												2	
CO2		3												3
CO3		3											3	
CO4			3		3									3

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule (for 26-week Sem)	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN445
Course Name	Mini Project-5
Desired Requisites:	Digital Signal Processing, Embedded System Design, VLSI Design, FPGA based System Design, Digital Image Processing, Power Electronics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	To provide students hands on experience on, troubleshooting, maintenance, fabrication, innovation, record keeping, documentation etc. thereby enhancing the skill and competency part of technical education
2	To create an industrial environment and culture within the institution.
3	To inculcate innovative thinking and practice based learning and thereby preparing students for their final year project.
4	To apply the knowledge gained to solve real life societal problems.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Choose, initiate and manage a minor project.	Understand
CO2	Propose research problem and present it in a clear and distinct manner through different oral, written and design techniques.	Apply
CO3	Construct the circuit using hardware and/or software.	Create
CO4	Execute the project and comment upon the results of it.	Analyze

List of Experiments / Lab Activities

Mini Project Description: The Mini Project is a team activity having 3-5 students in a team. This is electronic product design work with a focus on electronic circuit design. The theme of the Mini Project should be related to Electronics Engineering discipline based on comprehensive literature survey/ need analysis. **Mini Project should cater to a small system required in laboratory or real life.** The Mini Project may be a complete hardware or a combination of hardware and software. The Mini Project will involve the design, construction, and debugging of an electronic system approved by the department. Each student should conceive, design and develop the idea leading to a project/product. Each student must keep a project notebook/logbook. The project notebooks will be checked periodically throughout the semester, as part of in-semester-evaluation. The student should submit a soft bound report at the end of the semester. The final product as a result of Mini Project should be demonstrated at the time of examination.

Text Books

1	Charles Platt, "Make: Electronics", second edition, Maker Media, 2015
2	
3	
4	

References

1	
2	
3	

4	

Useful Links	
1	https://www.electronicshub.org/electronics-mini-projects-ideas/
2	https://www.elprocus.com/
3	https://www.electronicsforu.com/electronics-projects/hardware-diy/ece-projects
4	https://nevonprojects.com/engineering-projects-2/electronics-and-communication-projects/

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	3				2			3	2	2	2	2	2
CO2			3		2		2	2	2			2	2	2
CO3			3		2									3
CO4		2							3	3			2	2

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule (for 26-week Sem)	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level

Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total
Remember				
Understand	15	5		**20**
Apply	10	15	5	**30**
Analyze	5	10	15	**30**
Evaluate				
Create			20	**20**
Total	**30**	**30**	**40**	**100**

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AY 2022-23

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech Sem VII
Course Code	5EN411
Course Name	**Professional Elective 5: Microwave Engineering**
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 2**			

Course Objectives	
1	To understand the theoretical principles underlying microwave devices and networks
2	To introduce the various types of transmission lines and to discuss the losses associated
3	To instil knowledge on the properties of various microwave components
4	To deal with the microwave generation and microwave measurement techniques

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Classify the microwave frequencies and the waveguides that are used for various applications	Understand
CO2	Categories the propagation of signals through antenna	Analyze
CO3	Examine the active & passive microwave devices & components used in microwave communication systems	Apply
CO4	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	Analyze

Module	**Module Contents**	**Hours**
I	**Microwave Fundamentals and Electromagnetic field Theory:** Microwave regions and band designations, microwave devices, applications of microwaves, Interaction between electrons and fields, electron motion in electric, magnetic and electromagnetic field, electromagnetic plane waves	5
II	**Microwave Waveguide and Components:** Rectangular and circular waveguide, TE and TM modes, power transmission and power losses in waveguide, excitation modes in waveguide, microwave cavities, Microwave passive components—Tee junctions, magic tee, couplers, circulators, attenuators, phase shifters, bends, twists, corners, irises, windows. Scattering Matrix Parameters of microwave networks, S-matrix for E-plane Tee junction, S-matrix for H-plane Tee junctions, S-matrix for directional coupler.	5

III	**Microwave Tubes:** Limitations of conventional tubes, O and M type classification of microwave tubes, reentrant cavity, velocity modulation. O type tubes : Two cavity Klystron: Construction and principle of operation, velocity modulation and bunching process Applegate diagram. Reflex Klystron: Construction and principle of operation, velocity modulation and bunching process, Applegate diagram, Oscillating modes, o/p characteristics, efficiency, electronic & mechanical tuning. M-type tubes Magnetron: Construction and Principle of operation of 8 cavity cylindrical travelling wave magnetron, hull cutoff condition, modes of resonance, PI mode operation, o/p characteristics, Applications. Slow wave devices Advantages of slow wave devices, Helix TWT: Construction and principle of operation, Applications.	5
IV	**Microwave Solid State Devices:** Tunnel diode, PIN diode, Gunn diode, LSA diode, Read diode, IMPATT diode, TRAPATT diode, BARITT DIODE, Varactor Diode, solid state ruby laser, semiconductor laser.	5
V	**Microwave Measurements:** Measurement devices: Slotted line, Tunable detector, VSWR meter, Power Meter, S-parameter measurement, frequency measurements, Power measurement, Attenuation measurement, Phase shift measurement, VSWR measurement, Impedance measurement, Q of cavity resonator measurement	5
VI	**Microwave Strip Lines and Antenna** Micro-strip line, Slot line, Parallel strip line, advantages, Horn antenna, Dish Antenna, Micro-strip antenna	5

Text Books	
1	*"Microwave Devices and Circuits", Samuel* Y. Liao, PHI.
2	*"Microwave Engineering", 3rd Edition,* Manojit Mitra, Dhanpat Rai & Co
3	
4	

References	
1	*"Microwave Engineering",* D. M. Pozar, John Wiley
2	*"Electronics Communication Systems",* George Kennedy, Tata McGraw Hill.
3	
4	

Useful Links	
1	www.NPTEL.org
2	https://www.tutorialspoint.com/microwave_engineering/index.htm

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2		3												
CO3			3											2
CO4			3											

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													
CO2			2											
CO3			2											
CO4				2									1	1
1:Low, 2:Medium, 3:High														

Assessment (for Theory Course)
The assessment is based on 2 in-semester examinations in the form of T1 (Test-1) and T2 (Test-2) of 20 marks each. Also there shall be 1 End-Sem examination (ESE) of 60 marks. T1 shall be typically on modules 1 and 2, T2 based typically on modules 3, 4 and ESE shall be on all modules with nearly 50% weightage on modules 1 to 4 and 50% weightage on modules 5, 6.

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course					
Bloom's Taxonomy Level		**T1**	**T2**	**ESE**	**Total**
1	Remember				
2	Understand	5		10	15
3	Apply	10	10	25	45
4	Analyze				
5	Evaluate				
6	Create	5	10	25	40
Total		**20**	**20**	**60**	**100**

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech Semester II
Course Code	5EN412
Course Name	Professional Elective 5-Embedded Linux
Desired Requisites:	Computer Programming, Embedded System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	2 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 2**			

Course Objectives

1	To make students familiar with installation and use of the Linux/ Embedded Linux operating system.
2	To give exposure to system design using Embedded Linux as per the industry trends.
3	To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware.
4	To help the students design static and dynamic website for solving social problems using Embedded Linux.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Illustrate** Embedded Linux architecture and its working	*Understanding*
CO2	**Configure** Embedded System with Linux Environment	*Applying*
CO3	**Write** programs / scripts to configure and use internal / external peripherals of Embedded Linux Boards	*Applying*
CO4	**Design** and **develop** solution for social problems using the Embedded Linux	*Creating*

Module	**Module Contents**	**Hours**
I	**Introduction to Linux:** Introduction to Linux, Linux Distributions, Linux architecture, Linux Kernel, Hardware layer, System and Shell utility, Desktop Linux Installation and Configuration, Basic commands of Linux.	4
II	**Introduction to Embedded Linux:** Embedded Linux introduction, Why Embedded Linux? Linux vs. Embedded Linux, Embedded Linux Architecture, Components of Embedded Linux Systems, Classification of embedded Linux system, Tool chain, Embedded Linux Boot flow Process, Linux Kernel for Embedded Linux.	4
III	**Introduction embedded Linux Board**: Embedded Linux Boards, Raspberry Pi /Beagle Bone, Raspberry Pi / Beagle Bone - OS installation and configuration, Facilities in Embedded Linux Boards used in Industry/Market, Important Accessories of Linux boards available / used in industry.	5
IV	**Interfacing with embedded Linux board** Configure Network Setup & Remote access, Controlling GPIOs Interfacing various peripherals including, Interfacing Sensors, Camera etc.	5
V	**Embedded web server** Fundamentals of Web technology, Web server, Web Client, Server and client side scripting. Frontend / Backend programming and configuration, Installation of Web server on Embedded Linux boards and accessing them over intranet.	4
VI	**Case Study**: Web Based Applications, IoT Applications, Image Processing based	2

	applications	

Text Books	
1	*"Mastering Embedded Linux Programming"*, Second Edition, Chris Simmonds.
2	*"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux"* first Edition, Derek Molloy
3	*"Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux"* Derek Molloy
References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	https://www.geeksforgeeks.org/web-technology/
3	https://www.w3schools.com/
Useful Links	
1	https://www.linux.org/
2	https://www.raspberrypi.org/
3	https://www.raspberrypi.com/
4	https://www.coursera.org/

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN413
Course Name	Professional Elective 5-Analog CMOS IC Design
Desired Requisites:	Digital Electronics, Digital CMOS IC Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 4**			

Course Objectives

1	To **explain** the analog circuit concepts based on MOS devices in such a way to develop in students the insight and intuition towards MOS circuits.
2	To **organize** guest lectures and practical sessions with the help of industry persons.
3	To **deliver** the tips (or thumb rules) related with design of analog circuits throughout the course.
4	To **motivate** the students to develop lifelong/ self-learning attitude.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Analyze** MOS device circuits to derive the dependence of various electrical parameters analytically and graphically. (M1)	Analyze
CO2	**Develop** large signal and small signal models for single stage amplifiers and differential amplifiers using MOS transistors and derive the gain relationships. (M2, M3)	Apply
CO3	**Design** common source, common gate, common drain amplifier for given specifications. Further recognize their application under various typical situations. (M2, M3)	Design
CO4	**Analyze** large signal and small signal behaviour of differential amplifiers and compute the differential gain, common mode gain and CMRR. (M3)	Analyze
CO5	**Analyze** active current mirrors and explain the properties of differential pairs using such circuits as loads. (M5)	Analyze
CO6	**Design** 2-stage Op-Amp for given specifications. **Compute** the poles and zeros in the frequency response of the single stage amplifiers using time-constant method (M6)	Design

Module	**Module Contents**	**Hours**
I	**MOS Device Physics** MOS IV Characteristics, Second Order Effects, MOS device models (MOS device capacitance, MOS small signal model) MOS model parameters	8
II	**Single Stage Amplifier** Part I CS stage with resistance load, diode connected load, current source load, , CS stage with source, degeneration,	6
III	**Single Stage Amplifier** Part II source follower, common-gate stage, Cascode stage, folded cascade, choice of device models.	6
IV	**Differential Amplifiers** Basic difference pair, differential mode response, common mode response, Differential pair with MOS loads	6
V	**Passive and Active Current mirrors** Basic current mirrors, Cascode mirrors, active current mirrors.	7
VI	**Frequency Response** CS stage, Source follower, Common gate stage, Cascode stage and Difference pair. Design of 2-stage operational amplifier	7

Text Books	
1	Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, Second Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2017.
2	
3	
4	
References	
1	R. Jacob Baker, "*CMOS: Circuit Design, Layout and Simulation*", Wiley-Inter- science, (2008)
2	Allen, P.E. and Holberg, D.R., "*CMOS Analog Circuit Design*", Oxford University Press (2002)
3	
4	
Useful Links	
1	www.vlsi-expert.com,
2	www.testbench.in
3	www.asic-world.com
4	https://nptel.ac.in/courses/117/101/117101105/

CO-PO Mapping															
	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2	3												3	
CO2	2	3												3	
CO3			3											3	
CO4	2	3												3	
CO5	2	3												3	
CO6		2	3											3	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.															

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem
Course Code	5EN414
Course Name	**Professional Elective 5 Lab: Microwave Engineering Lab**
Desired Requisites:	Communication Engineering

Teaching Scheme (Hrs)		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2Hrs/week				
Interaction	-	**Credits: 1**			

Course Objectives

1	To understand the theoretical principles underlying microwave devices and networks
2	To instill knowledge on the properties of various microwave components
3	To deal with the microwave generation and microwave measurement techniques
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Classify the microwave frequencies and the waveguides that are used application	2
CO2	Categories the propagation of signals through antenna	4
CO3	Examine the active & passive microwave devices & components used in Microwave communication systems	4
CO4	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	4

List of Experiments / Lab Activities

List of Experiments:

1. Study of Microwave components and equipment
2. Study of V-I Characteristics of Gunn Diode
3. Reflex Klystron as source and plot its various modes
4. Verification of port characteristics of E-plane tee, H-plane tee & Magictree
5. Verification of port characteristics of Microwave Circulator and isolator, calculation of insertion loss and isolation loss
6. Verification of port characteristics of Directional coupler, calculation of coupling factor, insertion loss and directivity.
7. Power pattern of Horn Antenna
8. Power Patterns of different Antenna like Dipole, Yagi etc.
9. Study of slotted section with probe carriage. Measure the VSWR for various values of terminating impedances (open/short/matched termination).
10. To test and verify Microwave Integrated Circuits using Microstrip trainer kit and finds parameters, and plot the frequency response.

Text Books

1	**Textbooks:** *"Microwave Devices and Circuits", Samuel* Y. Liao, PHI.
2	*"Microwave Engineering", 3rd Edition,* Manojit Mitra, Dhanpat Rai & Co.
3	
4	

References	
1	*"Microwave Engineering",* D. M. Pozar, John Wiley.
2	*"Electronics Communication Systems",* George Kennedy, Tata McGraw Hill.
3	
4	

Useful Links	
1	
2	
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			3												
CO2				3											
CO3				3											
CO4			3												

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

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Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN415
Course Name	Professional Elective 5 Lab -Embedded Linux Lab
Desired Requisites:	Computer Programming, Embedded System Design

Teaching Scheme (Hrs)		Examination Scheme (Marks)			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2Hrs/week				
Interaction	-	**Credits: 1**			

Course Objectives	
1	To use Embedded Linux.
2	To learn system Architecture, configuration and Programming for Embedded Linux Based System.
3	To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware.
4	To facilitate the complete a mini-project involving embedded Linux hardware control/access through web, which can be used to solve some real life social/industrial problems.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**apply** programming skills to integrate hardware peripherals for Embedded Linux Board	*Applying*
CO2	**write** programs / scripts to configure and use internal / external peripherals of Embedded Linux Boards	*Applying*
CO3	**develop** and **demonstrate** small Embedded Linux based system	*Creating*

List of Experiments / Lab Activities

List of Experiments:

Experiments to revise an Embedded System Design
Experiment to study Linux distribution installation, configuration and basic commands of it.
Experiment to study Linux distribution installation, configuration for an Embedded Linux Board.
Experiment to configure and use network setup of an Embedded Linux Board
Experiment to access GPIO of an Embedded Linux Board to control components / devices interfaced to it.
Experiment to configure web server for an Embedded Linux board
Experiment to create web page, web site using programs / scripts.
Experiment to implement and access dynamic web page / web site for an Embedded Linux based system.
Experiment to configure and use an Embedded Linux board for image processing based applications
Mini project implementation and demonstration.

Text Books	
1	"Mastering Embedded Linux Programming", Second Edition, Chris Simmonds.
2	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux" first Edition, Derek Molloy
3	"Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux" Derek Molloy

References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	https://www.geeksforgeeks.org/web-technology/
3	https://www.w3schools.com/

Useful Links	
1	https://www.linux.org/

2	https://www.raspberrypi.org/
3	https://www.raspberrypi.com/
4	https://www.coursera.org/

CO-PO Mapping															
	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		2													
CO2				2		2									
CO3				2		2							1	1	
1:Low, 2:Medium, 3:High															

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.				
Assessment	**Based on**	**Conducted by**	**Typical Schedule (for 26-week Sem)**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

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Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN416
Course Name	Professional Elective 5 Lab- Analog CMOS IC Design Lab
Desired Requisites:	Digital Electronics, Digital CMOS IC Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	**Demonstrate** the flow of Cadence EDA tools for designing and simulating analog CMOS circuits.
2	**Develop** an insight into CMOS analog circuits and design single stage CS, CG, CD, differential amplifiers and 2-stsge Operational amplifier for given specifications.
3	**Explain** how to characterize the transistors for the voltage conditions seen by the circuit with goal of optimizing dimensions for given ID or trans-conductance.
4	**Prepare** the students for good documentation discipline.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Analyze** MOS transistors for targeted value of g_m or drain current for designing the physical dimensions and the required gate bias using Cadence EDA tools.	Analyze
CO2	**Demonstrate** the complete flow of Cadence tools from schematic to symbol generation to simulation for CS, CG, CD and differential amplifiers	Understand
CO3	**Build** and **simulate** the single stage amplifier circuits (CS, Source Follower, Cascode stage, differential pair etc.) using MOSFETs schematic design entry for various loads and relate the gain values with theoretical expressions.	Apply
CO4	**Design** differential pair circuits with active current mirror load for given gain and UGB.	Create
CO5	**Design**, **build** and **simulate** 2-stage operational amplifier for given pole frequencies and UGB with and without pole splitting and pole-zero compensation.	Create

List of Experiments / Lab Activities

List of Experiments:

Characterize nMOS transistors from schematic using Cadence tools.
Design, build and simulate single stage Common Source amplifier using resistive load and nMOS diode connected load (Gain and Frequency response). Compare the performance with pMOS diode connected load.
Design, build and simulate Common Source amplifiers with current source load. Compare the performance with already studied loads.
Design, build and simulate Common Source stage with source degeneration. (gain and frequency response) Compare the performance with and without source degeneration.
Design, build and simulate Source follower /Common Gate stage. Crosscheck the results of output impedance, gain, power dissipation against theoretical expectations.
Design, build and simulate cascode stage with different loads for the specified voltage gain and maximum power dissipation.
Design, build and simulate differential pair with specified tail current source and maximum full swing differential gain using, a)resistive load and b) pMOS current source load and compare the gain values. Cross-confirm the results against theoretical expectations.
Demonstrate the design of differential pair with active tail current source (replace the tail current source in Expt. 8 by a nMOS current source biased in saturation). Simulate for evaluating differential gain, common mode gain and CMRR.
Design, build and simulate differential amplifier (single ended output) with active current mirror load for the given specifications. Evaluate for CMRR, DC gain etc.
Demonstrate design of 2-stage operational amplifier for given UGB.

Text Books	
1	Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, Second Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2017.
2	
3	
4	

References	
1	R. Jacob Baker, "*CMOS: Circuit Design, Layout and Simulation*", Wiley-Inter- science, 2008.
2	Allen, P.E. and Holberg, D.R., "*CMOS Analog Circuit Design*", Second Edition, Oxford University Press, 2002.
3	
4	

Useful Links	
1	www.vlsi-expert.com
2	www.testbench.in
3	www.asic-world.com
4	https://nptel.ac.in/courses/117/101/117101105/

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	1			2	3									3	
CO2				2	3									3	
CO3			2	2	3									3	
CO4				3	3									3	
CO5				3	3									3	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Semester VIII
Course Code	5EN453
Course Name	Techno- Socio Activity
Desired Requisites:	Mini Project 1- 4

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture		**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	15	15	20	50
Practical	-				
Interaction	1Hrs/ Week	**Credits: 1**			

Course Objectives

1	To nurture the life skill qualities
2	To engage in independent and lifelong learning
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Use life skills	Apply
CO2	Select the proper opportunity in corporate life.	Analyze
CO3	Develop communication effectively with the engineering community and with society.	Create
CO4	Develop himself/ herself as successful Engineer	Create

Contents

To earn the credit, participation of the students in following activities (More than one activity) will be evaluated.

Internship: 15 days internship (Online/ Offline)

Co-curricular Activities : Co-Curricular activities include activities by chapters of professional societies like SAE, IEEE, ISTE, IET, Department Associations, Lab Development, Paper Presentation in National/International Conferences, Paper Publication in National/ International Journal, Model Building, Project competition, Entrepreneurship, Patenting, Participation in Dept level/ Institute level Technical club activities.

Extra - Curricular Activities: Extra-Curricular Activities include activities such as NSS, Unnat Bharat, Gymkhana Clubs, Cultural Fests (Inside or outside of the college), spots Event (Inside or outside of the college), Community Services, Social work, Activities in Alumni Association, Participation in Sports, Various Clubs of Institute, Intra and Inter Collegiate competitions . Participation in Department level/ Institute level club activities. (Activity conducted by club should be Technical- Ethics, Management, Professionalism/ skill/ Proficiency developments activities)

Course (Technical or fine arts) completed through **Continuing Education Program**
Any project completed which is helping the Electronics Engineering Department The performance of a student shall be monitored and evaluated by the Faculty-in-charge.

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1						3		3					2	
CO2							3							2
CO3										3				
CO4												3		2
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.				
Assessment	**Based on**	**Conducted by**	**Typical Schedule (for 26-week Sem)**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40
Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.				

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem. VII
Course Code	5EN446
Course Name	Project-I
Desired Requisites:	Mini Project

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	6 Hrs/Week				
Interaction	-	**Credits: 3**			

Course Objectives

1	**Explain** to survey and study the published literature on the assigned/ selected topic. The topic may be chosen from the problem assigned by the industry. The chosen topic may provide a solution to the electronics industry problem/ solution to societal needs.
2	**Explain** the use of methods/ methodology/ procedures/ software tools to carry out preliminary **Analysis**/ **Modelling**/ **Simulation**/ Experiment/ Design. It is expected to find out the feasibility of the project.
3	**Illustrate** the guidelines to write and **organize** the project report based on the study conducted for presentation to the department.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Explain** the purpose of the project and conceptual idea behind the project.	Understand
CO2	**Analyze** the journal/ conference/ research papers/ magazine articles and present the comparative study of similar work done by others.	Analyze
CO3	**Propose** a research problem/ problem undertaken as project-work and present it in a clear and distinct manner through different **design techniques** which meets the desired objectives of the project-work.	Create
CO4	**Prepare and Organize** written report on the study conducted/part of project-work (simulations/ technical design) completed for presentation before the department committee.	Apply

List of Experiments / Lab Activities

The objective of Project-I is to enable the student to take up investigative study in the broad field of Electronics Engineering, either fully theoretical/practical or involving both theoretical and practical work to be assigned by the Department on an individual basis or three/five students in a group, under the guidance of a Supervisor from the Department alone or jointly with a Supervisor/ Mentor from Industry. This is expected to provide a good initiation for the student(s) in R&D work.

The Projects may be chosen from the following areas/domains, but not limited to:

Embedded Systems/ VLSI Design
Electronic Communication Systems
Biomedical Electronics
Power Electronics/ Electric Vehicles
Robotics and Mechatronic Systems
Artificial Intelligence and Machine Learning
Applications of Electronics to Agriculture

Assessment: A demonstration and oral examination on the Project-I shall be conducted at the end of the semester.

Text Books

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.

2	
3	
4	

References	
1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
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4	

Useful Links	
1	https://ieeexplore.ieee.org
2	https://www.sciencedirect.com
3	https://www.elsevier.com
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3					3	2			2			2	2
CO2		3		3									3	3
CO3			3		2								3	3
CO4								2	3	3	3	2	2	2

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Walchand College of Engineering, Sangli

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Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5HS455
Course Name	Humanities -3 Project Management
Desired Requisites:	

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture		**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	15	15	20	50
Practical	-				
Interaction	1 Hrs/Week	**Credits: 1**			

Course Objectives

1	To prepare the students to manage projects by exploring both technical and managerial challenges and preparing the budget.
2	To make aware the students about leadership and ethical qualities in dealing with real life project
3	To induce qualities for working in interdisciplinary and cross functional teams with effective Communication skills, economical and managerial challenges and commercial management.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Grasp and perceive the project activities with respect to resources required and the constraint for feasibility or completion within time	Understand
CO2	Estimate and prepare budget for project completion, Understand commercial management	Analyze
CO3	Figure out and schedule the project and assess for controlling critical path networks	Evaluate
CO4		

Module	**Module Contents**	**Hours**
I	Introduction to Project Management.	2
II	Project Cost, Planning, feasibility, risk.	2
III	Critical Path Networks - Principles of Resource Scheduling.	2
IV	Executing and Controlling.	2
V	Commercial Management and various regulations.	2
VI	Study and use of software related to Project Management System.	3

Text Books

1	Dennis Lock , Project Management - Gower Publishing Limited, 2013
2	Samuel J. Mantel, Jr., Jack R. Meredith, Scott M. Shafer, Margaret M. Sutton , Project Management in Practice - JOHN WILEY & SONS, INC., 2011
3	B.C. Punmia and Khandelwal, Project Planning and Control with PERT and CPM, Lakshmi Publications Pvt. Ltd., 2001
4	HoraldKerzner, Project Management: A systems approach to planning, scheduling and controlling, John Wiley & Sons Inc., 2009
5	The factories act 1948 – Government of India 6. Meri Williams , The Principles of Project Management By – SitepointPvt Ltd., 2008

References

1	K. Nagarajan, Project Management, New Age Int., 2nd ed. 2004.
2	B.M.Naik, Project Management-Scheduling and Monitoring by PERT/CPM, 1984
3	William R Duncan, A guide to the project management body of knowledge, PMI Publications, 1996
4	
Useful Links	
1	https://www.apm.org.uk/resources/what-is-project-management/
2	https://www.projectmanager.com/project-management
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1								1					1	1
CO2									2					2
CO3							1						2	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN421
Course Name	TCP/IP and Advanced Protocol
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	20	20	60	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To develop an understanding of computer networking basics
2	be exposed to the TCP/IP protocol suite
3	To develop an understanding of different components of computer networks, various protocols, modern technologies and their applications.
4	To gain conceptual understanding of Software Defined Networks (SDN)

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Design a small TCP/IP Network	Apply
CO2	Identify security issues and suggest suitable solution	Analyze
CO3	Explain concept of cloud and its models.	Understand
CO4	Explain openflow challenges in SDN, and developments in SDN	Understand

Module	**Module Contents**	**Hours**
I	**Internet Protocol : IPv4 :** IP Datagram Formats - Data and Fragmentation - Address Masks- Prefixes- and Subnetworks - Network Address Translation (NAT) - IP Switching and Routing - Local Delivery and Loopbacks - Address Resolution Protocol ICMP.	8
II	**Transport layer protocols** UDP and TCP segments, comparison, TCP flow control, congestion control, error control.	6
III	**Application layer protocols:** Audio video streaming over IP (RTP,RTCP, SCTP), Application layer protocols, HTTP, SMTP, SNMP, FTP.	6
IV	**Security:** The Need of Security, Security Approaches, Principal of Security, Types of Attacks. Network Security: Brief Introduction to Firewalls, IP Security, Virtual Private Networks (VPN)	7
V	**Fundamental Cloud Computing :** Business Drivers - Technology Innovations - Basic Concepts and Terminology - Roles and Boundaries - Cloud Characteristics - Cloud Delivery Models - Cloud Deployment Models. Cloud-Enabling Technology	7
VI	**Software Defined Networking(SDN)**: Basics and Open flow, SDN Controller, SDN challenges, SDN and virtualization.	6

Text Books

1	" Computer Networks", B A Forouzan McGraw Hill Education 2016

2	Software defined Networking, Chuck Black Elsevier 2014
3	
4	
References	
1	Wayne Tomasi, “Introduction to Data Communication and Networking”, 1/e, Pearson Education .
2	Greg Tomsho, Ed Tittel, David Johnson. “Guide to Networking Essentials”, fifth edition, Thomson India Learning, 2007.
3	
4	
Useful Links	
1	https://www.cloudflare.com/en-in/learning/ddos/glossary/tcp-ip/
2	https://networkengineering.stackexchange.com/questions/63278/what-layers-of-the-tcp-ip-model-does-an-sdn-involve
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			2										2	
CO2		2												1
CO3		1												1
CO4	1	1												1

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

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AY 2022-23

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem. VIII
Course Code	5EN492
Course Name	Project-II
Desired Requisites:	Project - I

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**Lab ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	16 Hrs/Week				
Interaction	-	**Credits: 8**			

Course Objectives

1	Review and finalization of the approach to solve the problem relating to the assigned topic.
2	Finalizing objectives and expected outcomes of the project. Writing the technical specifications and product specifications of completed/ final project.
3	Detailed Analysis/Modelling/Simulation/Design/Problem Solving/Design of Experiments as required for the project-work.
4	Prepare a paper on project work for conference/ journal publication with suggested modifications and future of the project work.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Choose/ Experiment with the method/ methodology finalized/ designed to solve the problem undertaken as project.	Apply
CO2	Model/ Simulate/ Design/ Design the experiments to verify the expected results/ specifications of project.	Evaluate
CO3	Develop the final product/process, testing, results, conclusions and future direction.	Create
CO4	Write and publish a paper for Conference Presentation/Publication in Journals, if possible. Prepare a Project Report in the standard format for being evaluated by the department committee.	Apply
CO5	Prepare an action plan for conducting the investigation, sharing of activities during completion of project work, including team work.	Apply

List of Experiments / Lab Activities

It is expected that in-depth study of the topic assigned in the light of the report prepared under Project-I shall be continued as Project-II. The objective of Project-II is to enable the student to extend further the investigative study taken up under Project-I, either fully theoretical/practical or involving both theoretical and practical work, under the guidance of a Supervisor from the Department alone or jointly with a Supervisor from the Industry. It is expected to provide a good training for the student(s) in R&D work and technical leadership.

Assessment: The final product shall be a result of Project-I and Project-II and should be demonstrated at the time of examination. A demonstration and oral examination on the Project-II shall be conducted at the end of the semester.

Text Books

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	

References

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	
Useful Links	
1	https://ieeexplore.ieee.org
2	https://www.sciencedirect.com
3	https://www.elsevier.com
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	3		3	3	3	2					2	3	3
CO2		2	3	3	3							2	3	3
CO3			3		2	2	2	2			2	2	3	3
CO4								3	3	3	3	2	2	2
CO5									3		3			

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

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Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN431
Course Name	Professional Elective 6-System on Chip
Desired Requisites:	Embedded System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To design, optimize, and program a modern System-on-a-Chip.
2	To estimate key design metrics and requirements including area, latency, throughput, energy, power, predictability, and reliability.
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Discuss the functional and nonfunctional performance of the system early in the design process to support design decisions.	Understand
CO2	Apply concepts of System on Chip Design methodology for Logic and Analog Cores	Apply
CO3	Analyze hardware/software trade-offs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.	Analyze
CO4		

Module	**Module Contents**	**Hours**
I	**Introduction to the System Approach** Concept of system, importance of system architectures, introduction to SIMD, SSID, MIMD and MISD architectures, concept of pipelining and parallelism. Designing microprocessor /Microcontroller based system and embedded system	6
II	**Introduction to SOC** Differences between Embedded systems and SOCs. Introduction to busses used in SOCs, Introduction to AMBA bus, IBM's core connect bus, concept of PLB-processor local bus and OPB-on chip peripheral bus, System design issues in SOCs.	6
III	**Processors :** Concept of Soft embedded processors. Study of Microblaze RISC processor. Study of IBM's power PC	8
IV	**Programmable logic and FPGA Architecture :** Study of Latest FPGA Architecture. Study of features like embedded Block RAMs, multipliers, Digital clock management, CPU cores etc. Introduction to tools used for SOC design, Xilinx/ Altera embedded development kit	7
V	**Design Flow for SOC design** Using existing IP Blocks in SOC design, Designing new peripheral IP with AXI bus, Embedded programming with SOC.	6

VI	**Application Studies/ Case Studies** SOC system design example with Peripherals like USB, UART, Ethernet Etc. using latest FPGA. (Xilinx/ Altera tools) Eclipse IDE development tool for a full SOC system design with embedded C/C++ applications (Xilinx/ Altera tools)	7

Text Books	
1	Michael J. Flynn and Wayne Luk, "*Computer System Design System-on-Chip*", Wiley India Pvt. Ltd.
2	Steve Furber, "*ARM System on Chip Architecture*", 2nd Edition, 2000, Addison Wesley Professional.
3	
4	
References	
1	Ricardo Reis, "*Design of System on a Chip: Devices and Components*", 1st Edition, 2004, Springer
2	Jason Andrews, "*Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)*", Newnes, BK and CDROM.
3	Prakash Rashinkar, Peter Paterson and Leena Singh L, "*System on Chip Verification – Methodologies and Techniques*", 2001, Kluwer Academic Publishers.
Useful Links	
1	Core connect architecture at http://www.chips.IBM.com/products/coreconnect
2	EDK power PC tutorial at http://www.xilinx.com/EDK
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		2												
CO2			2										2	
CO3		2		2										

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Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech Sem VIII
Course Code	5EN432
Course Name	**Professional Elective 6: Digital System Engineering**
Desired Requisites:	ECAD , FPGA

Teaching Scheme		Examination Scheme (Marks)			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To understand the fundamental issues such as power, noise, signalling and timing associated with high speed digital systems.
2	To analyze the effect of parasitic of wires/interconnects in restricting the high speed performance of digital circuits and design the approaches to tackle this associate problem by using their engineering models.
3	To comprehend the different sources of interference (noise) in digital systems and apply engineering/statistical models of these to compute and compare bit error rates.
4	Understand the significance of signaling & timing issues and apply the knowledge of encoding a signal for error-free transfer of information (bits) from one location to another.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Understand Interconnects as design objects, Noise in digital systems and its impact to system operation	Understand
CO2	Analyze Timing and synchronization for functional operations and signalling	Analyze
CO3	Differentiate Power distribution schemes for low noise	Analyze
CO4	Explain Signal and signalling conventions for on-chip and off-chip communication	Understand

Module	Module Contents	Hours
I	**Transmission Lines:** Geometry and Electrical properties, Electrical models of wires (Ideal wire, Transmission line), Simple transmission lines (RC, lossless LC, lossy LRC transmission lines, Dielectric absorption), Special transmission lines (Multi drop buses, Balanced Transmission lines, Common and differential mode impedance, Isolated lines)	6
II	**Noise in Digital Systems:** Noise sources in a digital system, Power Supply Noise, Cross-talk, Inter-symbol Interference, Noise due to other sources (Alpha particles, Electro-magnetic Interference, Process variation, Thermal Noise, Shot Noise, Flicker or 1/f Noise), Managing noise.	6

III	**Signaling Conventions:** CMOS and Low swing current mode signaling system, Considerations in transmission system design, Signalling modes for transmission lines, Transmitter signalling methods, Receiver signal detection, Source termination, Under-terminated Drivers, Differential Signalling, Signalling over capacitive transmission medium, Signal encoding	6
IV	**Timing Conventions:** Conventional Synchronous system and closed loop pipelined system, considerations in timing design, Timing fundamentals, Timing properties of combinational logic and clock storage elements, Eye diagram, Encoding Timing (Signals and Events), Open loop synchronous timing, Closed loop timing, Phase locked loops, Clock Distribution	6
V	**Synchronization:** Synchronization Fundamentals, Applications of synchronization (Arbitration of asynchronous signals, Sampling asynchronous signals, Crossing clock domains), Synchronization failure and meta-stability, Synchronizer Design (Mesochronous, Plesiochronous, Periodic Asynchronous)	6
VI	**Power Distribution:** The power supply network (Local loads, Signal loads), Local Regulation, Logic loads and on-chip power supply distribution (Logic current profile, IR drops, Area Bonding, On-chip by-pass capacitor), Power supply isolation (Supply-supply isolation, Signal-supply isolation), Bypass capacitors, Power Distribution system	6

Text Books	
1	1. *"Digital System Engineering",* William Dally and John Poulton, Cambridge University Press, Reprint 2007

References	
1	1. *"High Speed Digital Design"- A Handbook of Black Magic,* Howard W. Johnson, Martin Graham, Prentice Hall PTR, Englewood Cliffs, NJ 0763.
2	*"High Speed Digital System Design: Interconnect Theory and Design Practices"* Stephen H. Hall, Garrett W. Hall, James A. McCall, Wiley-IEEE Press (ISBN: 978-0-471-36090-2

Useful Links	
1	https://engineeringtutorial.com/electrical-power-distribution/
2	https://www4.comp.polyu.edu.hk/~comp2322/Bit%20and%20Frame%20Synchronization%20Techiques.pdf
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3											
CO2					3									
CO3					3									
CO4				3										2

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AY 2022-23

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN433
Course Name	Professional Elective 7 :Radar and Navigation
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To learn Radar fundamentals and analysis of the radar signals.
2	To understand various technologies involved in the design of radar transmitters and receivers.
3	To learn various radars like MTI, Doppler and tracking radars and their comparison.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Demonstrate an understanding of the factors affecting the radar performance using Radar Range Equation	Understand
CO2	Analyze the principle of FM-CW radar	Analyze
CO3	Identify the different types of Radar Displays and their application in real time scenario	Apply
CO4	Demonstrate an understanding of the importance of Matched Filter Receivers in Radars	Understand

Module	**Module Contents**	**Hours**
I	**Basics of Radar**: Introduction, Maximum Unambiguous Range, Simple form of Radar Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications. Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation, Illustrative Problems. Radar Equation : SNR, Envelope Detector — False Alarm Time and Probability, Integration of Radar Pulses, Radar Cross Section of Targets (simple targets – sphere, cone-sphere), Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems.	8
II	**CW and Frequency Modulated Radar:** Doppler Effect, CW Radar — Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar. Illustrative Problems FM-CW Radar: Range and Doppler Measurement, Block Diagram and Characteristics, FM-CW altimeter, Multiple Frequency CW Radar	6
III	**MTI and Pulse Doppler Radar:** Introduction, Principle, MTI Radar with – Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancelers — Filter Characteristics, Blind Speeds, Double Cancellation, Staggered PRFs. Range Gated Doppler Filters. MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler Radar.	6

IV	**Tracking Radar**: Tracking with Radar, Sequential Lobing, Conical Scan, Monopulse Tracking Radar — Amplitude Comparison Monopulse (one- and two- coordinates), Phase Comparison Monopulse, Tracking in Range. Acquisition and Scanning Patterns. Comparison of Trackers.	6
V	**Detection of Radar Signals in Noise** : Introduction, Matched Filter Receiver – Response Characteristics and Derivation, Correlation Function and Cross- correlation Receiver, Efficiency of Non-matched Filters, Matched Fitter with Nonwhite Noise. **Radar Receivers** – Noise Figure and Noise Temperature. Displays — types. Duplexers — Branch type and Balanced type. Circulators as Duptexers. Introduction to Phased Array Antennas – Basic Concepts, Radiation Pattern, Beam Steering and Beam Width changes, Applications. Advantages and Limitations.	7
VI	**Radar clutter and basic navigational radar system** Introduction to Radar Clutter - Types, Surface clutter radar equation, Fundamentals of Navigation aids: Types of Navigation aids, ILS, DME, VOR, TACAN, MLS, LORAN, DECCA, OMEGA,	7

Text Books	
1	Skolnik, Merrill Ivan. Introduction to Radar Systems , TMH Special Indian Edition, 2nd Ed.. 2007. ISBN: 9780072881387
2	Raju, G. S. N.. Radar engineering. India, I.K. International Publishing House Pvt. Limited, 2008., ISBN: 9788190694216
3	
4	

References	
1	Mark A. Rkhards, James A. Scheer, William A. HoIm. Yesdee , Principles of Modem Radar: Basic Principles –, Scitech Publication, 2013, ISBN: 9781613532010
2	Radar Principles. India, Wiley India Pvt. Limited, 2007., ISBN: 9788126515271
3	
4	

Useful Links	
1	www.Nptel.ac.in
2	https://ocw.mit.edu/resources/res-ll-001-introduction-to-radar-systems
3	www.radartutorial.eu/index.en.html
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2	3													
CO3		3												2
CO4			3											

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech Sem VIII
Course Code	5EN434
Course Name	Professional Elective7- Data Analytics
Desired Requisites:	Data structures, Probability and statistics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	Understand fundamental algorithms and techniques used in Data Analytics
2	Learn various machine learning and data mining algorithms.
3	Learn Technological aspects like data management, scalable computation and visualization
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Identify** a meaningful pattern in data	Understand
CO2	Graphically **interpret** data	Analyze
CO3	**Implement** the analytic algorithms	Apply
CO4	**Select** decision support systems	Evaluate

Module	**Module Contents**	**Hours**
I	**Data Definitions and Analysis Techniques:** Elements, Variables, and Data categorization, Levels of Measurement, Data management and indexing, Introduction to statistical learning	7
II	**Descriptive Statistics:** Measures of central tendency, Measures of location of dispersions, Practice and analysis	6
III	**Statistical Techniques :** Basic analysis techniques, Statistical hypothesis generation and testing, Chi-Square test, t-Test	7
IV	**Statistical Analysis of Data:** Analysis of variance, Correlation analysis, Maximum likelihood test	7
V	**Data analysis techniques:** Regression analysis, Classification techniques, Clustering Association rules analysis	7
VI	**Case studies and projects:** Understanding business scenarios Feature engineering and visualization, Scalable and parallel computing, Sensitivity Analysis	6

Text Books

1	Ronald E. Walpole, Raymond H. Myers, Sharon L. Myers and Keying Ye, "Probability & Statistics for Engineers & Scientists" (9th Edn.), Prentice Hall Inc.
2	G James, D. Witten, T Hastie, and R. Tibshirani," An Introduction to Statistical Learning: with Applications in R, Springer, 2013"

3	
4	
References	
1	Anna Maria Paganoni and Piercesare Secchi, Advances in Complex Data Modeling and Computational Methods in Statistics, Springer, 2013
2	Mohammed J. Zaki, Wagner Meira, Data Mining and Analysis, Cambridge, 2012
3	
4	
Useful Links	
1	https://www.educba.com/data-science/data-science-tutorials/data-analytics-basics/
2	https://datacrunchcorp.com/data-analytics-tutorial-for-beginners/
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		2												
CO2			2											2
CO3					2									
CO4													2	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.														

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2022-23

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech Sem VIII
Course Code	5EN435
Course Name	**Professional Elective 8: Satellite Communication**
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To prepare students to excel in basic knowledge of satellite communication principles
2	To train the students with a basic knowledge of link design of satellite with a design examples
3	To provide students with solid foundation in orbital mechanics and launches for the satellite communication
4	To provide better understanding of multiple access systems and earth station technology

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Explain the satellite communication principles	Understand
CO2	Apply link design of satellite	Apply
CO3	Design various satellite applications	Apply

Module	**Module Contents**	**Hours**
I	**Module 1: Communication Satellite:** Orbit and Description: A Brief history of satellite Communication, Satellite Frequency Bands, Satellite Systems, Applications, Orbital Period and Velocity, effects of Orbital Inclination, Azimuth and Elevation, Coverage angle and slant Range, Eclipse, Orbital Perturbations, Placement of a Satellite in a Geo-Stationary orbit..	6
II	**Module 2: Satellite Sub-Systems:** Attitude and Orbit Control system, TT &C subsystem, Attitude Control subsystem, Power systems, Communication subsystems, Satellite Antenna Equipment. Satellite Link: Basic Transmission Theory, System Noise Temperature and G/T ratio, Basic Link Analysis, Interference Analysis, Design of satellite Links for a specified C/N, (With and without frequency Re-use), Link Budget.	6
III	**Module 3: Propagation effects:** Introduction, Atmospheric Absorption, Cloud Attenuation, Tropospheric and lonospeheric Scintillation and Low angle fading, Rain induced attenuation, rain induced cross polarization interference.	6
IV	**Module 4: Multiple Access:** Frequency DivisIon Multiple Access (FDMA) – Intermodujation Calculation of C/N, Time Division Multiple Access (TDMA) – Frame Structure, Burst Structure, Satellite Switched TDMA, On-board Processing, Demand Assignment Multiple Access (DAMA) — Types of Demand Assignment, Characteristics, CDMA Spread Spectrum Transmission and Reception.	6

V	**Module 5: Earth Station Technology:** Transmitters, Receivers, Antennas, Tracking Systems, Terrestrial Interface, Power Test Methods, Lower Orbit Considerations	6
VI	**Module 6: Satellite Navigation and GPS System**s: Radio and Satellite Navigation, GPS Position Location Principles, GPS Receivers, GPS C/A Code Accuracy, Differential GPS.	6

Text Books	
1	Roddy, Dennis. Satellite communications. India, McGraw-Hill Education, 2006, ISBN: 9780071462983
2	Bostian, Charles W., and Pratt, Timothy. Satellite Communications. United Kingdom, Wiley, 2019, ISBN: 978-1-119-48217-8
3	
4	
References	
1	Richharia, Madhavendra, "Satellite Communication Systems: Design Principles", United Kingdom, Macmillan Education, Limited, 2017., ISBN: 9781349149643
2	Rao, K. N. Raja. "Fundamentals of Satellite Communication" India, Prentice Hall of India, 2004, ISBN: 9788120324015
3	
4	
Useful Links	
1	https://www.tutorialspoint.com/satellite_communication/satellite_communication_link_budget.htm
2	https://www.itu.int/en/ITU-R/space/workshops/2016-small-sat/Documents/Link_budget_uvigo.pdf
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2	3		3											
CO3			3											2
CO4														

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Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem VIII
Course Code	5EN436
Course Name	Professional Elective 8- Internet of Things
Desired Requisites:	Sensors and Instrumentation, Embedded System

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To provide understanding of the Internet of Things concepts.
2	To demonstrate various IoT communication protocols.
3	To understand applications of Internet of Things and its usefulness for society.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Explain IoT building blocks	Understand
CO2	Compare various IoT connectivity and communication technologies	Analyze
CO3	Design applications for solution building in IoT domain	Apply

Module	**Module Contents**	**Hours**
I	**Overview of Internet of Things** : Introduction of IoT, Network Configuration and addressing, IoT sensors and actuators	6
II	**Connectivity and Communication Technologies for IoT** : IEEE 802.15.4, 6LowPAN, RFID, WiFi, Bluetooth, Zigbee, Wireless HART for IoT, MQTT, CoAP, XMPP, AMQP	8
III	**Sensor networks** :Target tracking, MWSN, UWSN, Stationary and Mobile WSN, UAV Networks	8
IV	**Machine to Machine Communication** : M2M Features, Node types, Ecosystem, various M2M platforms	6
V	**Sensor Cloud** : Limitations of WSN, Architecture, workflow, target tracking, Localization Techniques, LoRaWAN Protocol ,virtual sensor, caching in sensor cloud, performance, pricing	6
VI	**IoT Applications** : Smart cities, Smart Homes, Smart Agriculture, Smart Energy, Smart vehicles	6

Text Books	
1	"Introduction to Industrial Internet of Things and Industry 4.0" Sudip Misra, Chandana Roy, Anandarup Mukherjee 2021
2	
3	

References	
1	D.E. Comer "Internetworking with TCP/IP", Vol. I (4th Edition), II, III (PHI)
2	"Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud" Pearson Education

Useful Links	
1	https://onlinecourses.nptel.ac.in/noc21_cs17/preview
2	

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3										2	
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